CY7C0850AV,CY7C0851V/CY7C0851AV
CY7C0852V/CY7C0852AV
CY7C0853V/CY7C0853AV

FLEx36™ 3.3 V 32K/64K/128K/256K x 36 Synchronous Dual-Port RAM

Features

- True dual-ported memory cells that allow simultaneous access of the same memory location
- Synchronous pipelined operation
- Organization of 1-Mbit, 2-Mbit, 4-Mbit, and 9-Mbit devices
- Pipelined output mode allows fast operation
- 0.18-micron Complimentary metal oxide semiconductor (CMOS) for optimum speed and power
- High-speed clock to data access
- 3.3 V low power
  - Active as low as 225 mA (typ)
  - Standby as low as 55 mA (typ)
- Mailbox function for message passing
- Global master reset
- Separate byte enables on both ports
- Commercial and industrial temperature ranges
- IEEE 1149.1-compatible Joint test action group (JTAG) boundary scan
- 172-Ball fine-pitch ball grid array (FBGA) (1 mm pitch) (15 mm × 15 mm)
- 176-Pin thin quad plastic flatpack (TQFP) (24 mm × 24 mm × 1.4 mm)
- Counter wrap around control
  - Internal mask register controls counter wrap-around
  - Counter-interrupt flags to indicate wrap-around
  - Memory block retransmit operation
- Counter readback on address lines
- Mask register readback on address lines
- Dual chip enables on both ports for easy depth expansion

Functional Description

The FLEx36™ family includes 1M, 2M, 4M, and 9M pipelined, synchronous, true dual-port static RAMs that are high-speed, low-power 3.3 V CMOS. Two ports are provided, permitting independent, simultaneous access to any location in memory. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address, and data lines allow for minimal setup and hold time.

During a Read operation, data is registered for decreased cycle time. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address, the counter increments the address internally (more details to follow). The internal Write pulse width is independent of the duration of the R/$\overline{W}$ input signal. The internal Write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE0}$ or LOW on CE1 for one clock cycle powers down the internal circuitry to reduce the static power consumption. One cycle with chip enables asserted is required to reactivate the outputs.

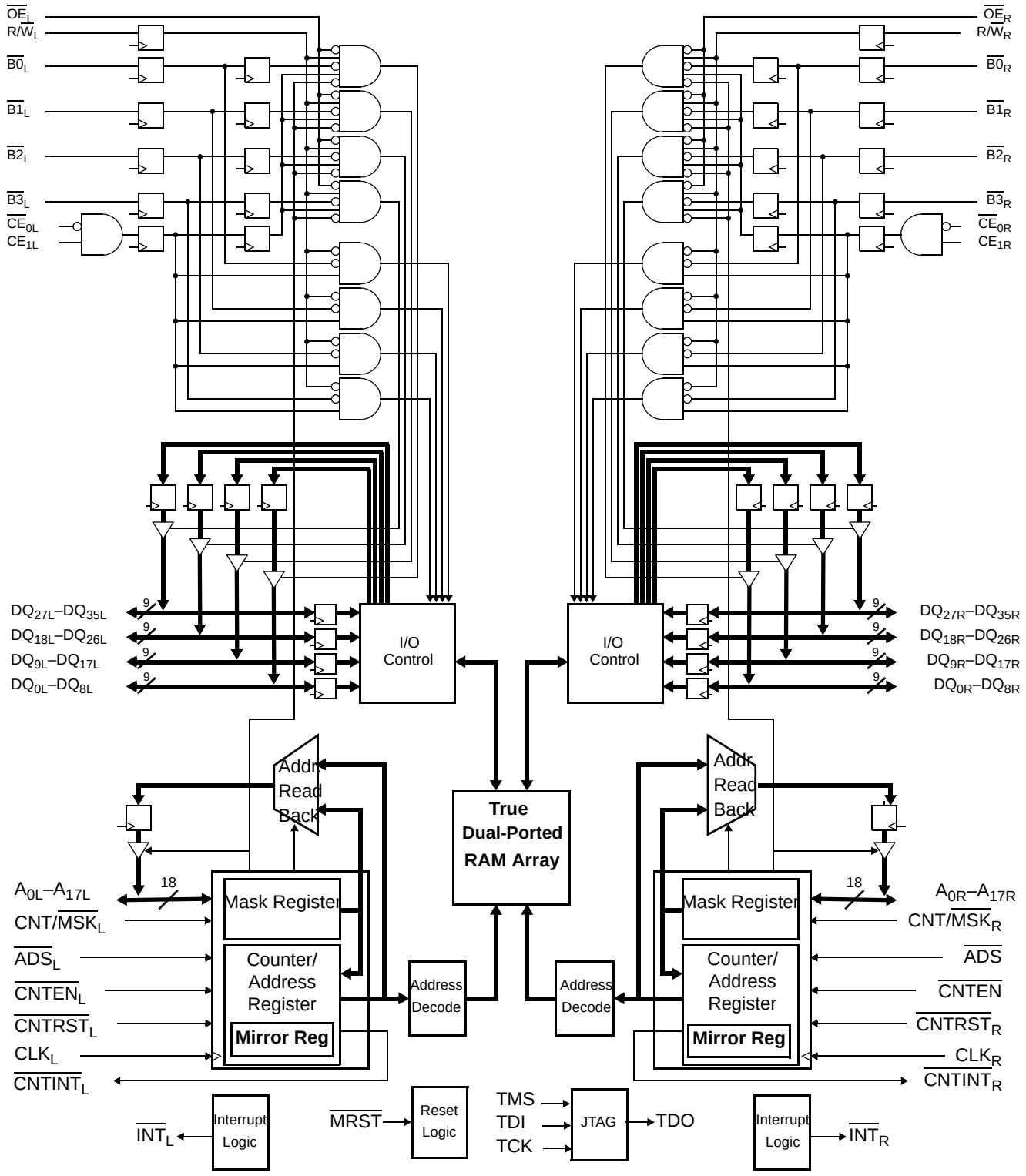
Additional features include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around, counter interrupt (CNTINT) flags, readback of mask register value on address lines, retransmit functionality, interrupt flags for message passing, JTAG for boundary scan, and asynchronous Master Reset ($\overline{MRST}$).

The CY7C0853V/CY7C0853AV device in this family has limited features. Please see See “Address Counter and Mask Register Operations” on page 9. for details.

Table 1. Product Selection Guide

Density	1-Mbit (32K x 36)	2-Mbit (64K x 36)	4-Mbit (128K x 36)	9-Mbit (256K x 36)
Part number	CY7C0850AV	CY7C0851V/ CY7C0851AV	CY7C0852V/ CY7C0852AV	CY7C0853V/ CY7C0853AV
Max. speed (MHz)	167	167	167	133
Max. access time - clock to data (ns)	4.0	4.0	4.0	4.7
Typical operating current (mA)	225	225	225	270
Package	176TQFP 172FBGA	176TQFP 172FBGA	176TQFP 172FBGA	172FBGA

Logic Block Diagram [1]



Note
1. 9M device has 18 address bits, 4M device has 17 address bits, 2M device has 16 address bits, and 1M device has 15 address bits.

Contents

Pin Configurations

Figure 1. 172-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DQ32L	DQ30L	$\overline{\text{CNTINTL}}$	VSS	DQ13L	VDD	DQ11L	DQ11R	VDD	DQ13R	VSS	$\overline{\text{CNTINTR}}$	DQ30R	DQ32R
B	A0L	DQ33L	DQ29L	DQ17L	DQ14L	DQ12L	DQ9L	DQ9R	DQ12R	DQ14R	DQ17R	DQ29R	DQ33R	A0R
C	NC	A1L	DQ31L	DQ27L	$\overline{\text{INTL}}$	DQ15L	DQ10L	DQ10R	DQ15R	$\overline{\text{INTR}}$	DQ27R	DQ31R	A1R	NC
D	A2L	A3L	DQ35L	DQ34L	DQ28L	DQ16L	VSS	VSS	DQ16R	DQ28R	DQ34R	DQ35R	A3R	A2R
E	A4L	A5L	CE1L	$\overline{\text{B0L}}$	VDD	VSS			VDD	VDD	$\overline{\text{B0R}}$	CE1R	A5R	A4R
F	VDD	A6L	A7L	$\overline{\text{B1L}}$	VDD					VSS	$\overline{\text{B1R}}$	A7R	A6R	VDD
G	$\overline{\text{OEL}}$	$\overline{\text{B2L}}$	$\overline{\text{B3L}}$	$\overline{\text{CE0L}}$	CY7C0850AV CY7C0851V/CY7C0851AV CY7C0852V/CY7C0851AV						$\overline{\text{CE0R}}$	$\overline{\text{B3R}}$	$\overline{\text{B2R}}$	$\overline{\text{OER}}$
H	VSS	R/$\overline{\text{W}}$L	A8L	CLKL							CLKR	A8R	R/$\overline{\text{W}}$R	VSS
J	A9L	A10L	VSS	$\overline{\text{ADSL}}$	VSS					VDD	$\overline{\text{ADSR}}$	$\overline{\text{MRST}}$	A10R	A9R
K	A11L	A12L	A15L[2]	$\overline{\text{CNTRSTL}}$	VDD	VDD			VSS	VDD	$\overline{\text{CNTRSTR}}$	A15R[2]	A12R	A11R
L	CNT/$\overline{\text{MSKL}}$	A13L	$\overline{\text{CNTENL}}$	DQ26L	DQ25L	DQ19L	VSS	VSS	DQ19R	DQ25R	DQ26R	$\overline{\text{CNTENR}}$	A13R	CNT/$\overline{\text{MSKR}}$
M	A16L[2]	A14L	DQ22L	DQ18L	TDI	DQ7L	DQ2L	DQ2R	DQ7R	TCK	DQ18R	DQ22R	A14R	A16R[2]
N	DQ24L	DQ20L	DQ8L	DQ6L	DQ5L	DQ3L	DQ0L	DQ0R	DQ3R	DQ5R	DQ6R	DQ8R	DQ20R	DQ24R
P	DQ23L	DQ21L	TDO	VSS	DQ4L	VDD	DQ1L	DQ1R	VDD	DQ4R	VSS	TMS	DQ21R	DQ23R

Note
2. For CY7C0851V/CY7C0851AV, pins M1 and M14 are NC. For CY7C0850AV, pins K3, K12 M1, and M14 are NC

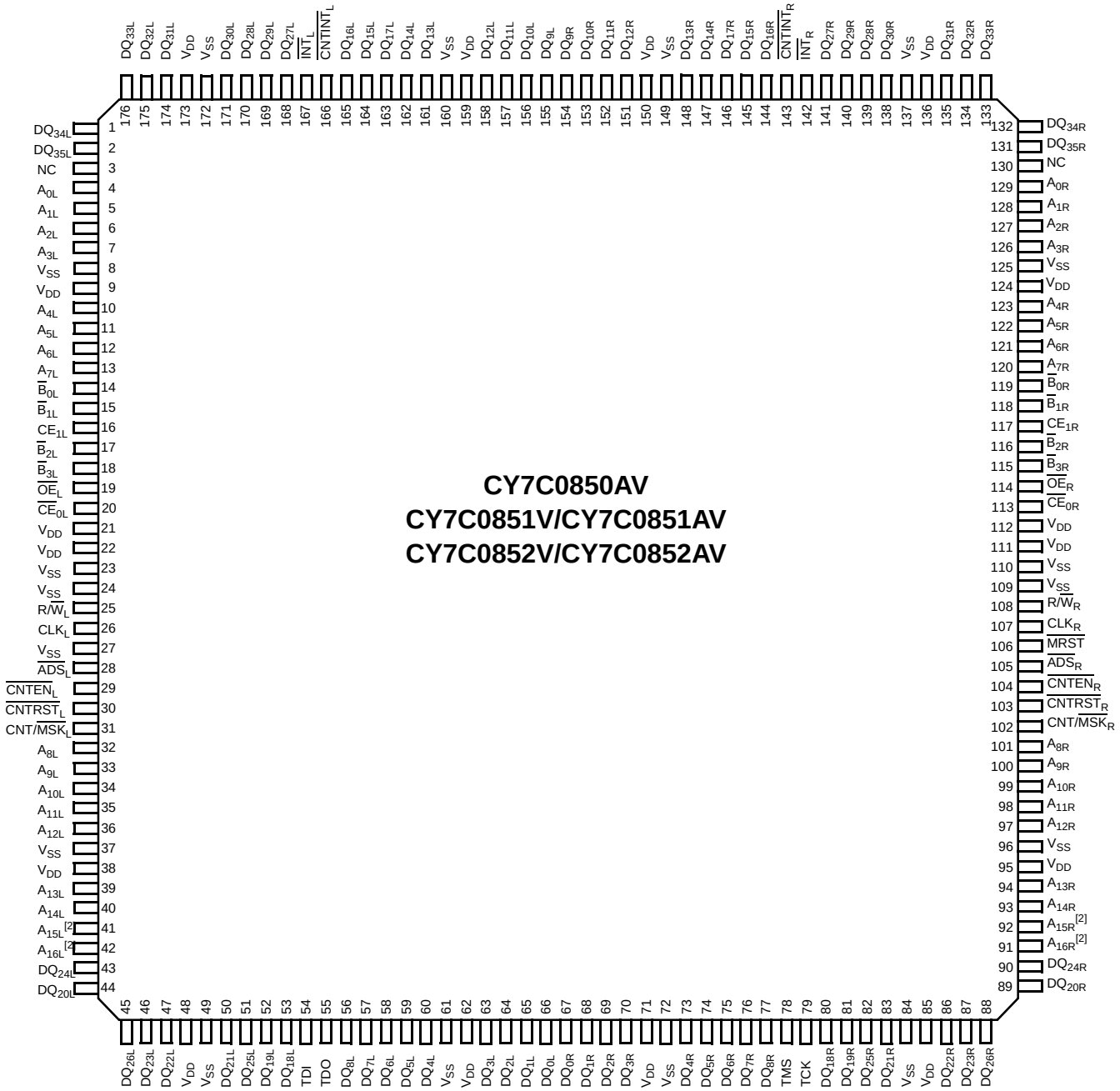
Pin Configurations (continued)

Figure 2. 172-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DQ32L	DQ30L	NC	VSS	DQ13L	VDD	DQ11L	DQ11R	VDD	DQ13R	VSS	NC	DQ30R	DQ32R
B	A0L	DQ33L	DQ29L	DQ17L	DQ14L	DQ12L	DQ9L	DQ9R	DQ12R	DQ14R	DQ17R	DQ29R	DQ33R	A0R
C	A17L	A1L	DQ31L	DQ27L	$\overline{\text{INTL}}$	DQ15L	DQ10L	DQ10R	DQ15R	$\overline{\text{INTR}}$	DQ27R	DQ31R	A1R	A17R
D	A2L	A3L	DQ35L	DQ34L	DQ28L	DQ16L	VSS	VSS	DQ16R	DQ28R	DQ34R	DQ35R	A3R	A2R
E	A4L	A5L	VDD	$\overline{\text{B0L}}$	VDD	VSS			VDD	VDD	$\overline{\text{B0R}}$	VDD	A5R	A4R
F	VDD	A6L	A7L	$\overline{\text{B1L}}$	VDD					VSS	$\overline{\text{B1R}}$	A7R	A6R	VDD
G	$\overline{\text{OEL}}$	$\overline{\text{B2L}}$	$\overline{\text{B3L}}$	VSS	CY7C0853V/CY7C0853AV						VSS	$\overline{\text{B3R}}$	$\overline{\text{B2R}}$	$\overline{\text{OER}}$
H	VSS	R/$\overline{\text{WL}}$	A8L	CLKL							CLKR	A8R	R/$\overline{\text{WR}}$	VSS
J	A9L	A10L	VSS	VSS	VSS					VDD	VSS	$\overline{\text{MRST}}$	A10R	A9R
K	A11L	A12L	A15L	VDD	VDD	VDD			VSS	VDD	VDD	A15R	A12R	A11R
L	VDD	A13L	VSS	DQ26L	DQ25L	DQ19L	VSS	VSS	DQ19R	DQ25R	DQ26R	VSS	A13R	VDD
M	A16L	A14L	DQ22L	DQ18L	TDI	DQ7L	DQ2L	DQ2R	DQ7R	TCK	DQ18R	DQ22R	A14R	A16R
N	DQ24L	DQ20L	DQ8L	DQ6L	DQ5L	DQ3L	DQ0L	DQ0R	DQ3R	DQ5R	DQ6R	DQ8R	DQ20R	DQ24R
P	DQ23L	DQ21L	TDO	VSS	DQ4L	VDD	DQ1L	DQ1R	VDD	DQ4R	VSS	TMS	DQ21R	DQ23R

Pin Configurations (continued)

Figure 3. 176-Pin Thin Quad Flat Pack (TQFP) (Top View)



Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{17L}[3]	A_{0R}–A_{17R}[3]	**Address inputs**.
ADS_L[4]	ADS_R[4]	**Address strobe input**. Used as an address qualifier. This signal should be asserted LOW for the part using the externally supplied address on the address pins and for loading this address into the burst address counter.
$\overline{CE0_L}$[4]	$\overline{CE0_R}$[4]	**Active LOW chip enable input**.
$CE1_L$[4]	$CE1_R$[4]	**Active HIGH chip enable input**.
CLK_L	CLK_R	**Clock signal**. Maximum clock input rate is f_{MAX}.
$CNTEN_L$[4]	$CNTEN_R$[4]	**Counter enable input**. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. The increment is disabled if ADS or CNTRST are asserted LOW.
$CNTRST_L$[4]	$CNTRST_R$[4]	**Counter reset input**. Asserting this signal LOW resets to zero the unmasked portion of the burst address counter of its respective port. CNTRST is not disabled by asserting ADS or CNTEN.
$CNT/\overline{MSK}_L$[4]	$CNT/\overline{MSK}_R$[4]	**Address counter mask register enable input**. Asserting this signal LOW enables access to the mask register. When tied HIGH, the mask register is not accessible and the address counter operations are enabled based on the status of the counter control signals.
DQ_{0L}–DQ_{35L}	DQ_{0R}–DQ_{35R}	**Data bus input/output**.
$\overline{OE}_L$	$\overline{OE}_R$	**Output enable input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INT}$L	$\overline{INT}$R	**Mailbox interrupt flag output**. The mailbox permits communications between ports. The upper two memory locations can be used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$CNTINT_L$[4]	$\overline{CNTINT}_R$[4]	**Counter interrupt output**. This pin is asserted LOW when the unmasked portion of the counter is incremented to all “1s.”
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write enable input**. Assert this pin LOW to write to, or HIGH to Read from the dual port memory array.
$\overline{B}_{0L}$–$\overline{B}_{3L}$	$\overline{B}_{0R}$–$\overline{B}_{3R}$	**Byte select inputs**. Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{MRST}$		**Master reset input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A $\overline{MRST}$ operation is required at power up.
TMS		**JTAG test mode select input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.
TDI		**JTAG test data input**. Data on the TDI input is shifted serially into selected registers.
TCK		**JTAG test clock input**.
TDO		**JTAG test data output**. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP.
V_{SS}		**Ground inputs**.
V_{DD}		**Power inputs**.

Notes
3. 9M device has 18 address bits, 4M device has 17 address bits, 2M device has 16 address bits, and 1M device has 15 address bits
4. These pins are not available for CY7C0853V/CY7C0853AV device.

Master Reset

The FLEx36 family devices undergo a complete reset by taking its MRST input LOW. The MRST input can switch asynchronously to the clocks. The MRST initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). The MRST also forces the Mailbox Interrupt (INT) flags and the Counter Interrupt (CNTINT) flags HIGH. The MRST must be performed on the FLEx36 family devices after power up.

Mailbox Interrupts

The upper two memory locations may be used for message passing and permit communications between ports. *Table 2* shows the interrupt operation for both ports of CY7C853V/CY7C0853AV. The highest memory location, 3FFFF is the mailbox for the right port and 3FFFE is the mailbox for the left port. *Table 2* shows that in order to set the $\overline{INT}_R$ flag, a Write operation by the left port to address 3FFFF asserts $\overline{INT}_R$ LOW. At least one byte has to be active for a Write to generate an interrupt. A valid Read of the 3FFFF location by the right port resets $\overline{INT}_R$ HIGH. At least one byte has to be active in order for a Read to reset the interrupt. When one port Writes to the other port's mailbox, the INT of the port that the mailbox belongs to is asserted LOW. The INT is reset when the owner (port) of the mailbox Reads the contents of the mailbox. The interrupt flag is set in a flow-thru mode (that is it follows the clock edge of the writing port). Also, the flag is reset in a flow-thru mode (that is it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. And each port can write to its own mailbox without setting the interrupt. If an application does not require message passing, INT pins should be left open.

Table 2. Interrupt Operation Example [5, 6, 7, 8, 9]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L-17L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R-17R}	$\overline{INT}_R$
Set right $\overline{INT}_R$ flag	L	L	3FFFF	X	X	X	X	L
Reset right $\overline{INT}_R$ flag	X	X	X	X	H	L	3FFFF	H
Set left $\overline{INT}_L$ flag	X	X	X	L	L	L	3FFFE	X
Reset left $\overline{INT}_L$ flag	H	L	3FFFE	H	X	X	X	X

Table 3. Address Counter and Counter-Mask Register Control Operation (Any Port) [10, 11]

CLK	$\overline{MRST}$	CNT/$\overline{MSK}$	$\overline{CNTRST}$	$\overline{ADS}$	$\overline{CNTEN}$	Operation	Description
X	L	X	X	X	X	Master reset	Reset address counter to all 0s and mask register to all 1s.
⎍	H	H	L	X	X	Counter reset	Reset counter unmasked portion to all 0s.
⎍	H	H	H	L	L	Counter load	Load counter with external address value presented on address lines.
⎍	H	H	H	L	H	Counter readback	Read out counter internal value on address lines.
⎍	H	H	H	H	L	Counter increment	Internally increment address counter value.
⎍	H	H	H	H	H	Counter hold	Constantly hold the address value for multiple clock cycles.
⎍	H	L	L	X	X	Mask reset	Reset mask register to all 1s.
⎍	H	L	H	L	L	Mask load	Load mask register with value presented on the address lines.
⎍	H	L	H	L	H	Mask readback	Read out mask register value on address lines.
⎍	H	L	H	H	X	Reserved	Operation undefined

Notes
5. 9 M device has 18 address bits, 4M device has 17 address bits, 2M device has 16 address bits, and 1M device has 15 address bits
6. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the CLK and can be deasserted after that. Data is out after the following CLK edge and is three-stated after the next CLK edge.
7. $\overline{OE}$ is "Don't Care" for mailbox operation.
8. At least one of $\overline{B0}$, $\overline{B1}$, $\overline{B2}$, or $\overline{B3}$ must be LOW.
9. A16x is a NC for CY7C0851V/CY7C0851AV, therefore the Interrupt Addresses are FFFF and EFFF; A16x and A15x are NC for CY7C0850AV, therefore the Interrupt Addresses are 7FFF and 6FFF.
10. "X" = "Don't Care," "H" = HIGH, "L" = LOW.
11. Counter operation and mask register operation is independent of chip enables.

Address Counter and Mask Register Operations

This section[12] describes the features only apply to CY7C0850AV/CY7C0851V/0851AV/CY7C0852V/0852AV devices, but not to the CY7C0853V/0853AV device. Each port of these devices has a programmable burst address counter. The burst counter contains three registers: a counter register, a mask register, and a mirror register.

The **counter register** contains the address used to access the RAM array. It is changed only by the Counter Load, Increment, Counter Reset, and by master reset (MRST) operations.

The **mask register** value affects the Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The mask register is changed only by the Mask Load and Mask Reset operations, and by the MRST. The mask register defines the counting range of the counter register. It divides the counter register into two regions: zero or more “0s” in the most significant bits define the masked region, one or more “1s” in the least significant bits define the unmasked region. Bit 0 may also be “0,” masking the least significant counter bit and causing the counter to increment by two instead of one.

The mirror register is used to reload the counter register on increment operations (see “retransmit,” below). It always contains the value last loaded into the counter register, and is changed only by the Counter Load operation, and by the MRST.

Table 3 on page 8 summarizes the operation of these registers and the required input control signals. The MRST control signal is asynchronous. All the other control signals in Table 3 on page 8 (CNT/MSK, CNTRST, ADS, CNTEN) are synchronized to the port’s CLK. All these counter and mask operations are independent of the port’s chip enable inputs (CE0 and CE1).

Counter enable ($\overline{\text{CNTEN}}$) inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast, interleaved memory applications. A port’s burst counter is loaded when the port’s address strobe ($\overline{\text{ADS}}$) and $\overline{\text{CNTEN}}$ signals are LOW. When the port’s $\overline{\text{CNTEN}}$ is asserted and the $\overline{\text{ADS}}$ is deasserted, the address counter increments on each LOW to HIGH transition of that port’s clock signal. This will Read/Write one word from/into each successive address location until $\overline{\text{CNTEN}}$ is deasserted. The counter can address the entire memory array, and loops back to the start. Counter reset ($\overline{\text{CNTRST}}$) is used to reset the unmasked portion of the burst counter to 0s. A counter-mask register is used to control the counter wrap.

Counter Reset Operation

All unmasked bits of the counter are reset to “0.” All masked bits remain unchanged. The mirror register is loaded with the value of the burst counter. A Mask Reset followed by a Counter Reset will reset the counter and mirror registers to 00000, as will master reset (MRST).

Counter Load Operation

The address counter and mirror registers are both loaded with the address value presented at the address lines.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. Readback is pipelined; the address is valid t_{CA2} after the next rising edge of the port’s clock. If address readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) is three-stated. Figure 4 on page 11 shows a block diagram of the operation.

Counter Increment Operation

Once the address counter register is initially loaded with an external address, the counter can internally increment the address value, potentially addressing the entire memory array. Only the unmasked bits of the counter register are incremented. The corresponding bit in the mask register must be a “1” for a counter bit to change. The counter register is incremented by 1 if the least significant bit is unmasked, and by 2 if it is masked. If all unmasked bits are “1,” the next increment wraps the counter back to the initially loaded value. If an Increment results in all the unmasked bits of the counter being “1s,” a counter interrupt flag ($\overline{\text{CNTINT}}$) is asserted. The next Increment returns the counter register to its initial value, which was stored in the mirror register. The counter address can instead be forced to loop to 00000 by externally connecting $\overline{\text{CNTINT}}$ to $\overline{\text{CNTRST}}$.[13] An increment that results in one or more of the unmasked bits of the counter being “0” deasserts the counter interrupt flag. The example in Figure 5 on page 12 shows the counter mask register loaded with a mask value of 0003Fh unmasking the first 6 bits with bit “0” as the LSB and bit “16” as the MSB. The maximum value the mask register can be loaded with is 1FFFFh. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 8h. The base address bits (in this case, the 6th address through the 16th address) are loaded with an address value but do not increment once the counter is configured for increment operation. The counter address starts at address 8h. The counter increments its internal address value till it reaches the mask register value of 3Fh. The counter wraps around the memory block to location 8h at the next count. $\overline{\text{CNTINT}}$ is issued when the counter reaches its maximum value.

Counter Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Notes
12. This section describes the CY7C0852V/CY7C0852AV, which have 17 address bits and a maximum address value of 1FFFF. The CY7C0851V/CY7C0851AV has 16 address bits, register lengths of 16 bits, and a maximum address value of FFFF. The CY7C0850AV has 15 address bits, register lengths of 15 bits, and a maximum address value of 7FFF.
13. $\overline{\text{CNTINT}}$ and $\overline{\text{CNTRST}}$ specs are guaranteed by design to operate properly at speed grade operating frequency when tied together.

Counter Interrupt

The counter interrupt ($\overline{\text{CNTINT}}$) is asserted LOW when an increment operation results in the unmasked portion of the counter register being all “1s.” It is deasserted HIGH when an Increment operation results in any other value. It is also de-asserted by Counter Reset, Counter Load, Mask Reset and Mask Load operations, and by $\overline{\text{MRST}}$.

Retransmit

Retransmit is a feature that allows the Read of a block of memory more than once without the need to reload the initial address. This eliminates the need for external logic to store and route data. It also reduces the complexity of the system design and saves board space. An internal “mirror register” is used to store the initially loaded address counter value. When the counter unmasked portion reaches its maximum value set by the mask register, it wraps back to the initial value stored in this “mirror register.” If the counter is continuously configured in increment mode, it increments again to its maximum value and wraps back to the value initially stored into the “mirror register.” Thus, the repeated access of the same data is allowed without the need for any external logic.

Mask Reset Operation

The mask register is reset to all “1s,” which unmasks every bit of the counter. Master reset ($\overline{\text{MRST}}$) also resets the mask register to all “1s.”

Mask Load Operation

The mask register is loaded with the address value presented at the address lines. Not all values permit correct increment operations. Permitted values are of the form $2^n - 1$ or $2^n - 2$. From the most significant bit to the least significant bit, permitted values have zero or more “0s,” one or more “1s,” or one “0.” Thus 1FFFF, 003FE, and 00001 are permitted values, but 1F0FF, 003FC, and 00000 are not.

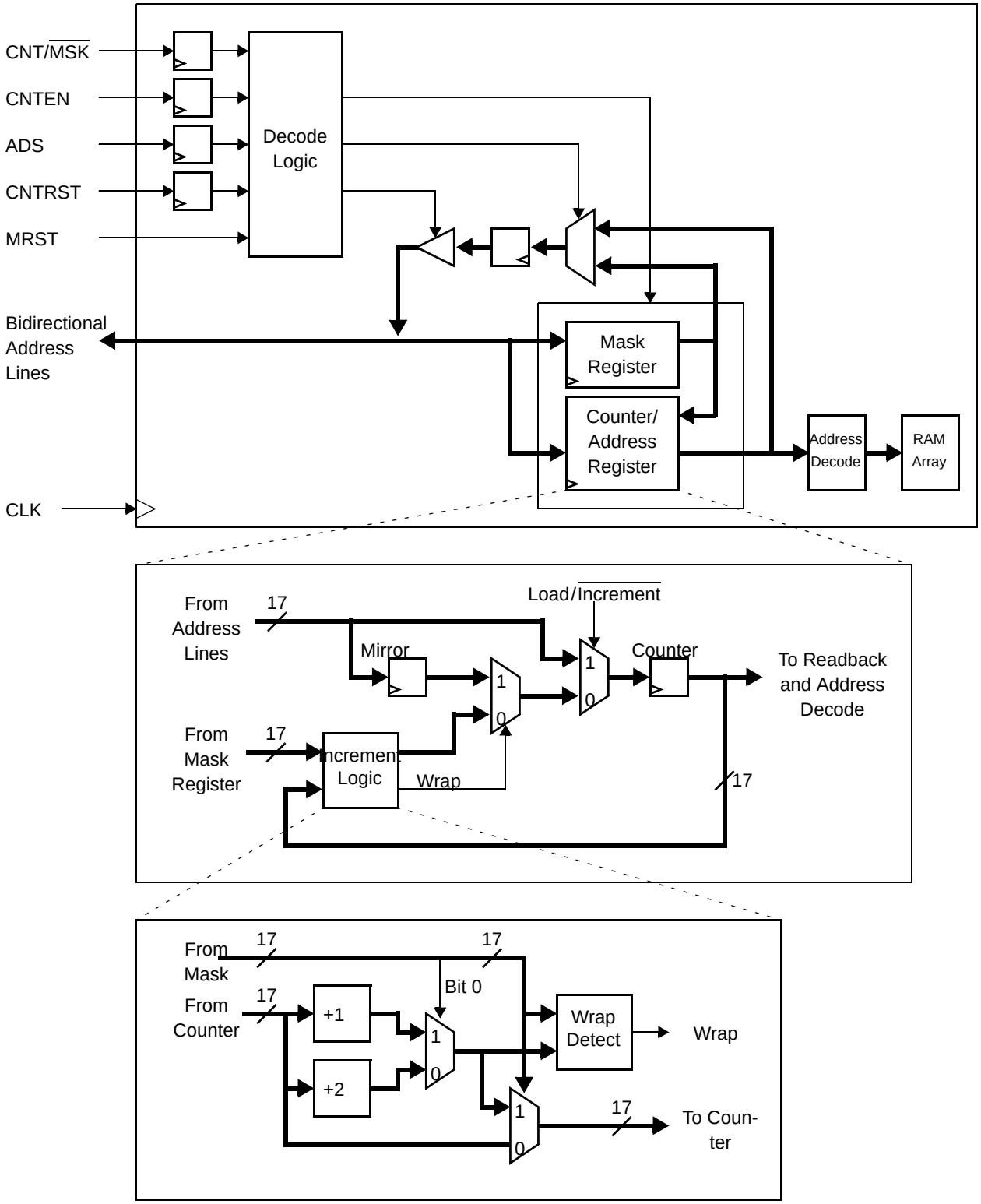
Mask Readback Operation

The internal value of the mask register can be read out on the address lines. Readback is pipelined; the address is valid t_{CM2} after the next rising edge of the port’s clock. If mask readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) is three-stated. Figure 4 on page 11 shows a block diagram of the operation.

Counting by Two

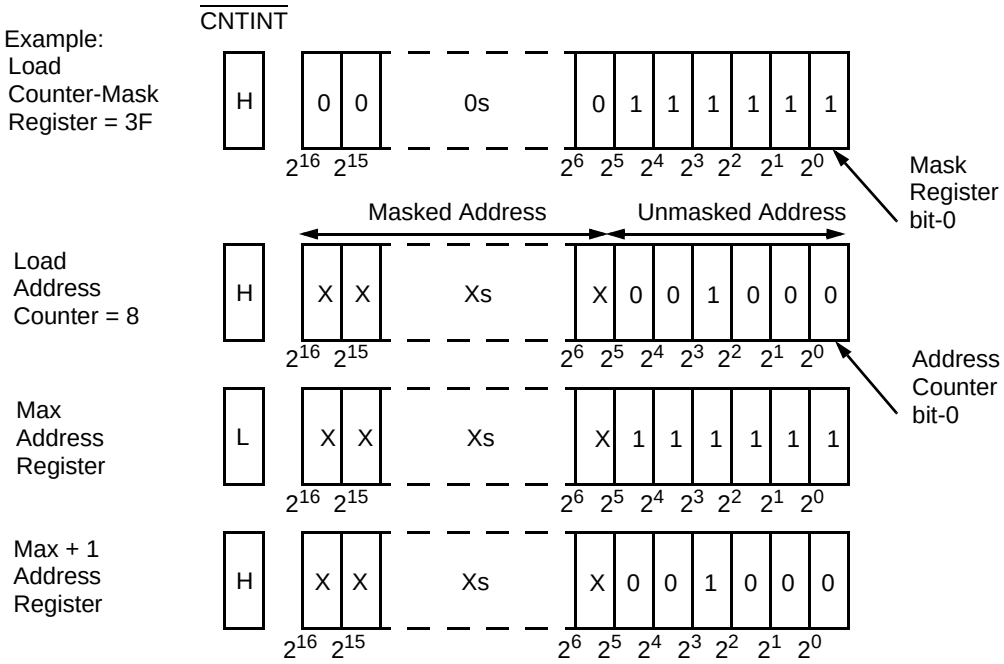
When the least significant bit of the mask register is “0,” the counter increments by two. This may be used to connect the CY7C0850AV/CY7C0851V/0851AV/CY7C0852V/CY7C0852AV as a 72-bit single port SRAM in which the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 72-bit data in even memory locations, and the other half in odd memory locations.

Figure 4. Counter, Mask, and Mirror Logic Block Diagram [14]



Note
14. 9M device has 18 address bits, 4M device has 17 address bits, 2M device has 16 address bits, and 1M device has 15 address bits

Figure 5. Programmable Counter-Mask Register Operation [15, 16]



Notes
15. 9M device has 18 address bits, 4M device has 17 address bits, 2M device has 16 address bits, and 1M device has 15 address bits
16. The “X” in this diagram represents the counter upper bits

IEEE 1149.1 Serial Boundary Scan (JTAG) [17]

The CY7C0850AV / CY7C0851V / CY7C0851AV / CY7C0852V /CY7C0852AV / CY7C0853V / CY7C0853AV incorporates an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1-compliant TAPs. The TAP operates using JEDEC-standard 3.3 V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the devices, and may be performed while the devices are operating. An MRST must be performed on the devices after power-up.

Performing a Pause/Restart

When a SHIFT-DR PAUSE-DR SHIFT-DR is performed the scan chain outputs the next bit in the chain twice. For example, if the value expected from the chain is 1010101, the device outputs a 11010101. This extra bit causes some testers to report an erroneous failure for the devices in a scan test. Therefore the tester should be configured to never enter the PAUSE-DR state.

Table 4. Identification Register Definitions

Instruction Field	Value	Description
Revision number (31:28)	0h	Reserved for version number.
Cypress device ID (27:12)	C001h	Defines Cypress part number for the CY7C0851V/0851AV
	C002h	Defines Cypress part number for the CY7C0852V/0852AV and CY7C0853V/0853AV
	C092h	Defines Cypress part number for the CY7C0850AV
Cypress JEDEC ID (11:1)	034h	Allows unique identification of the DP family device vendor.
ID register presence (0)	1	Indicates the presence of an ID register.

Table 5. Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n[18]

Table 6. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all CY7C0851AV/CY7C0852AV/ CY7C0853AV output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
NBSRST	1100	Resets the non-boundary scan logic. Places BYR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Notes
17. Boundary scan is IEEE 1149.1-compatible. See “Performing a Pause/Restart” for deviation from strict 1149.1 compliance.
18. See details in the device BSDL files.

Maximum Ratings

Exceeding maximum ratings[19] may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with Power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.5 V to + 4.6 V

DC voltage applied to Outputs in High-Z state ..... –0.5 V to V_{DD} + 0.5 V

DC input voltage ..... –0.5 V to V_{DD} + 0.5 V[20]

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2000 V (JEDEC JESD22-A114-2000B)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0 °C to +70 °C	3.3 V ± 165 mV
Industrial	–40 °C to +85 °C	3.3 V ± 165 mV

Electrical Characteristics

Over the Operating Range

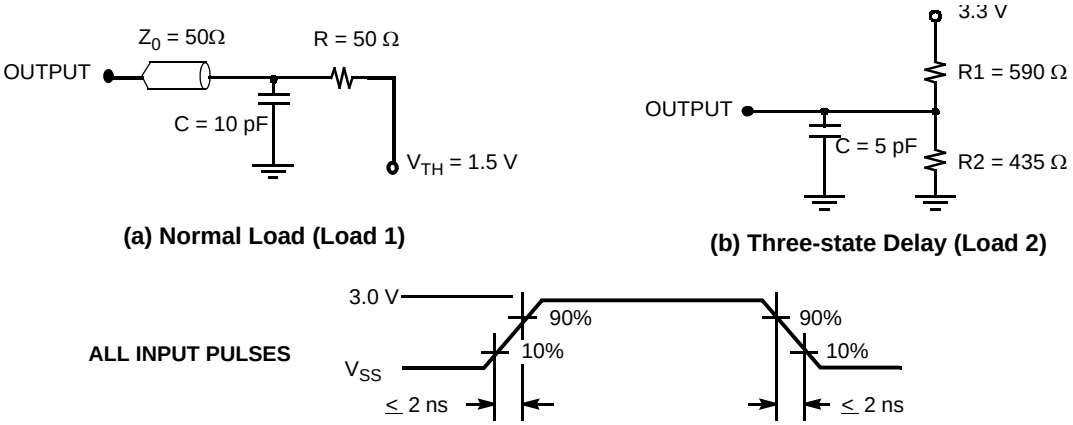
Parameter	Description		-167			-133			-100			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage (V_{DD} = Min., I_{OH}= –4.0 mA)		2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage (V_{DD} = Min., I_{OL}= +4.0 mA)		–		0.4	–		0.4			0.4	V
V_{IH}	Input HIGH voltage		2.0		–	2.0		–	2.0		–	V
V_{IL}	Input LOW voltage		–		0.8	–		0.8			0.8	V
I_{OZ}	Output leakage current		–10		10	–10		10	–10		10	µA
I_{IX1}	Input leakage current except TDI, TMS, $\overline{MRST}$		–10		10	–10	–	10	–10	–	10	µA
I_{IX2}	Input leakage current TDI, TMS, $\overline{MRST}$		–0.1		1.0	–0.1	–	1.0	–0.1	–	1.0	mA
I_{CC}	Operating current for (V_{DD} = Max.,I_{OUT} = 0 mA), Outputs disabled	CY7C0850AV CY7C0851V/AV CY7C0852V/AV	–	225	300	–	225	300	–	–	–	mA
		CY7C0853V/ CY7C0853AV	–	–	–	–	270	400	–	200	310	
I_{SB1}[22]	Standby current (both ports TTL level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}		–	90	115	–	90	115	–	90	115	mA
I_{SB2}[22]	Standby current (one port TTL level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}		–	160	210	–	160	210	–	160	210	mA
I_{SB3}[22]	Standby current (both ports CMOS level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD}$ – 0.2 V, f = 0		–	55	75	–	55	75	–	55	75	mA
I_{SB4}[22]	Standby current (one port CMOS level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}		–	160	210	–	160	210	–	160	210	mA
I_{SB5}	Operating current (V_{DD} = Max, I_{OUT} = 0 mA, f = 0) Outputs disabled	CY7C0853V/ CY7C0853AV	–	–	–	–	70	100	–	70	100	mA

Capacitance

Part Number[21]	Parameter	Description	Test Conditions	Max	Unit
CY7C0850AV,CY7C0851V CY7C0851AV, CY7C0852V, CY7C0852AV	C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V	13	pF
	C_{OUT}	Output capacitance		10	pF
CY7C0853V,CY7C0853AV	C_{IN}	Input capacitance		22	pF
	C_{OUT}	Output capacitance		20	pF

Notes
19. The voltage on any input or I/O pin can not exceed the power pin during power up.
20. Pulse width < 20 ns.
21. C_{OUT} also references $C_{I/O}$.
22. I_{SB1}, I_{SB2}, I_{SB3} and I_{SB4} are not applicable forCY7C0853V/ CY7C0853AV because it can not be powered down by using chip enable pins.

Figure 6. AC Test Load and Waveforms



(a) Normal Load (Load 1)

(b) Three-state Delay (Load 2)

Switching Characteristics

Over the Operating Range

Parameter	Description	-167		-133				-100		Unit
		CY7C0850AV CY7C0851V/AV CY7C0852V/AV		CY7C0850AV CY7C0851V/AV CY7C0852V/AV		CY7C0853V CY7C0853AV		CY7C0853V CY7C0853AV		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX2}	Maximum operating frequency	–	167	–	133	–	133	–	100	MHz
t_{CYC2}	Clock cycle time	6.0	–	7.5	–	7.5	–	10.0	–	ns
t_{CH2}	Clock HIGH time	2.7	–	3.0	–	3.0	–	4.0	–	ns
t_{CL2}	Clock LOW time	2.7	–	3.0	–	3.0	–	4.0	–	ns
t_R[23]	Clock rise time	–	2.0	–	2.0	–	2.0	–	3.0	ns
t_F[23]	Clock fall time	–	2.0	–	2.0	–	2.0	–	3.0	ns
t_{SA}	Address setuptime	2.3	–	2.5	–	2.5	–	3.0	–	ns
t_{HA}	Address hold time	0.6	–	0.6	–	0.6	–	0.6	–	ns
t_{SB}	Byte select setup time	2.3	–	2.5	–	2.5	–	3.0	–	ns
t_{HB}	Byte select hold time	0.6	–	0.6	–	0.6	–	0.6	–	ns
t_{SC}	Chip enable setup time	2.3	–	2.5	–	NA	–	NA	–	ns
t_{HC}	Chip enable hold time	0.6	–	0.6	–	NA	–	NA	–	ns
t_{SW}	R/$\overline{W}$ setup time	2.3	–	2.5	–	2.5	–	3.0	–	ns
t_{HW}	R/$\overline{W}$ hold time	0.6	–	0.6	–	0.6	–	0.6	–	ns
t_{SD}	Input data setup time	2.3	–	2.5	–	2.5	–	3.0	–	ns
t_{HD}	Input data hold time	0.6	–	0.6	–	0.6	–	0.6	–	ns
t_{SAD}	$\overline{ADS}$ setup time	2.3	–	2.5	–	NA	–	NA	–	ns
t_{HAD}	$\overline{ADS}$ hold time	0.6	–	0.6	–	NA	–	NA	–	ns
t_{SCN}	$\overline{CNTEN}$ setup time	2.3	–	2.5	–	NA	–	NA	–	ns
t_{HCN}	$\overline{CNTEN}$ hold time	0.6	–	0.6	–	NA	–	NA	–	ns
t_{SRST}	$\overline{CNTRST}$ setup time	2.3	–	2.5	–	NA	–	NA	–	ns
t_{HRST}	$\overline{CNTRST}$ hold time	0.6	–	0.6	–	NA	–	NA	–	ns
t_{SCM}	CNT/$\overline{MSK}$ setup time	2.3	–	2.5	–	NA	–	NA	–	ns
t_{HCM}	CNT/$\overline{MSK}$ hold time	0.6	–	0.6	–	NA	–	NA	–	ns

Note

23. Except JTAG signals (t_r and t_f < 10 ns [max.]).

Switching Characteristics

Over the Operating Range (continued)

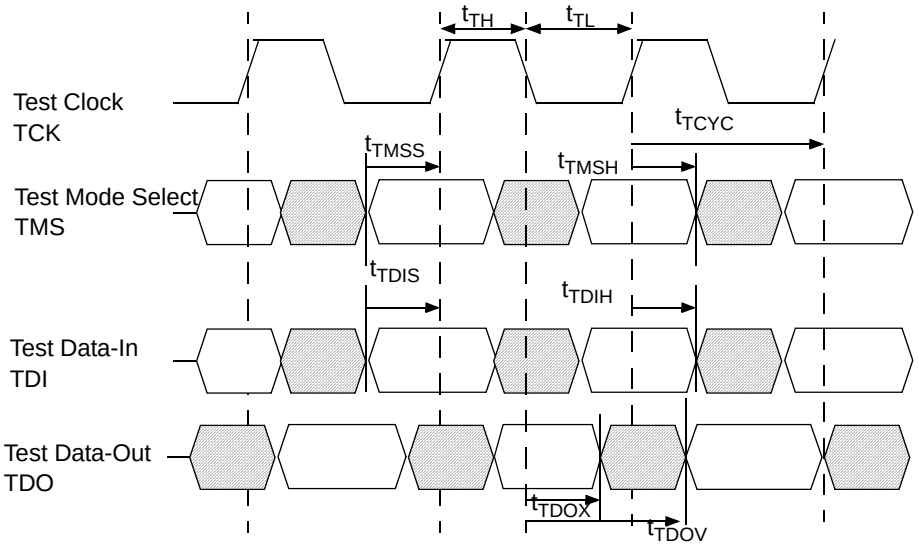
Parameter	Description	-167		-133				-100		Unit
		CY7C0850AV CY7C0851V/AV CY7C0852V/AV		CY7C0850AV CY7C0851V/AV CY7C0852V/AV		CY7C0853V CY7C0853AV		CY7C0853V CY7C0853AV		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{OE}	Output enable to data valid	–	4.0	–	4.4	–	4.7	–	5.0	ns
t_{OLZ}[24, 25]	$\overline{OE}$ to Low Z	0	–	0	–	0	–	0	–	ns
t_{OHZ}[24, 25]	$\overline{OE}$ to High Z	0	4.0	0	4.4	0	4.7	0	5.0	ns
t_{CD2}	Clock to data valid	–	4.0	–	4.4	–	4.7	–	5.0	ns
t_{CA2}	Clock to counter address valid	–	4.0	–	4.4	–	NA	–	NA	ns
t_{CM2}	Clock to mask register readback valid	–	4.0	–	4.4	–	NA	–	NA	ns
t_{DC}	Data output hold after clock HIGH	1.0	–	1.0	–	1.0	–	1.0	–	ns
t_{CKHZ}[24, 25]	Clock HIGH to output High Z	0	4.0	0	4.4	0	4.7	0	5.0	ns
t_{CKLZ}[24, 25]	Clock HIGH to output Low Z	1.0	4.0	1.0	4.4	1.0	4.7	1.0	5.0	ns
t_{SINT}	Clock to $\overline{INT}$ set time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10	ns
t_{RINT}	Clock to $\overline{INT}$ reset time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ set time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ reset time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
Port to Port Delays										
t_{CCS}	Clock to clock skew	5.2	–	6.0	–	6.0	–	8.0	–	ns
Master Reset Timing										
t_{RS}	Master reset pulse width	7.0	–	7.5	–	7.5	–	10.0	–	ns
t_{RSS}	Master reset setup time	6.0	–	6.0	–	6.0	–	8.5	–	ns
t_{RSR}	Master reset recovery time	6.0	–	7.5	–	7.5	–	10.0	–	ns
t_{RSF}	Master reset to outputs inactive	–	10.0	–	10.0	–	10.0	–	10.0	ns
$t_{RSCNTINT}$	Master reset to counter interrupt flag reset time	–	10.0	–	10.0	–	NA	–	NA	ns

Notes
24. This parameter is guaranteed by design, but it is not production tested.
25. Test conditions used are Load 2.

JTAG Timing

Parameter	Description	167/133/100		Unit
		Min	Max	
f_{JTAG}	Maximum JTAG TAP controller frequency	–	10	MHz
t_{TCYC}	TCK clock cycle time	100	–	ns
t_{TH}	TCK clock HIGH time	40	–	ns
t_{TL}	TCK clock LOW Time	40	–	ns
t_{TMSS}	TMS setup to TCK clock rise	10	–	ns
t_{TMSH}	TMS hold after TCK clock rise	10	–	ns
t_{TDIS}	TDI setup to TCK clock rise	10	–	ns
t_{TDIH}	TDI hold after TCK clock rise	10	–	ns
t_{TDOV}	TCK clock LOW to TDO valid	–	30	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns

Figure 7. JTAG Switching Waveform



Switching Waveforms

Figure 8. Master Reset

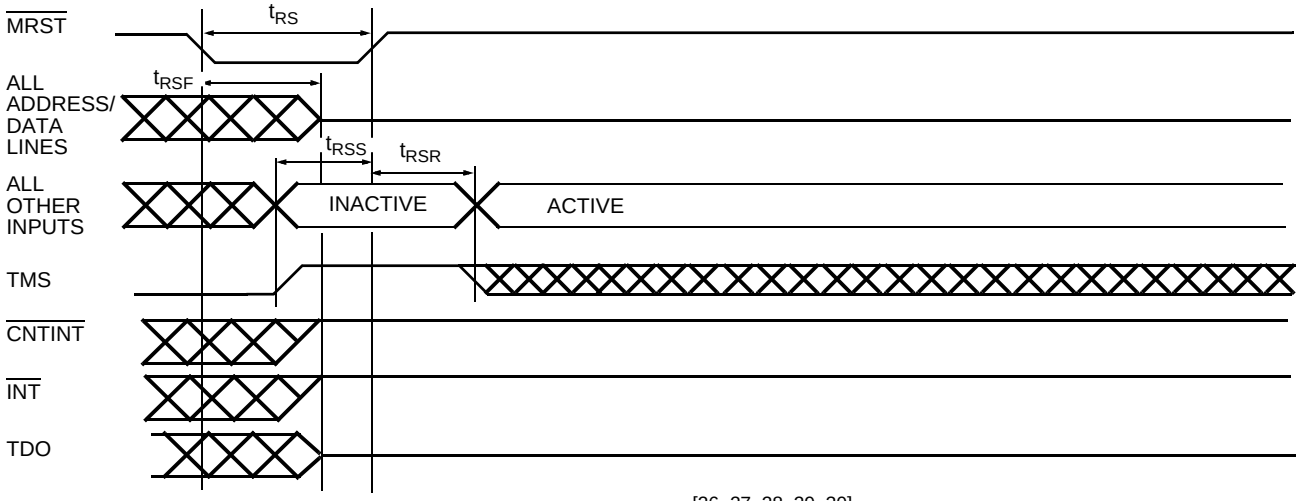
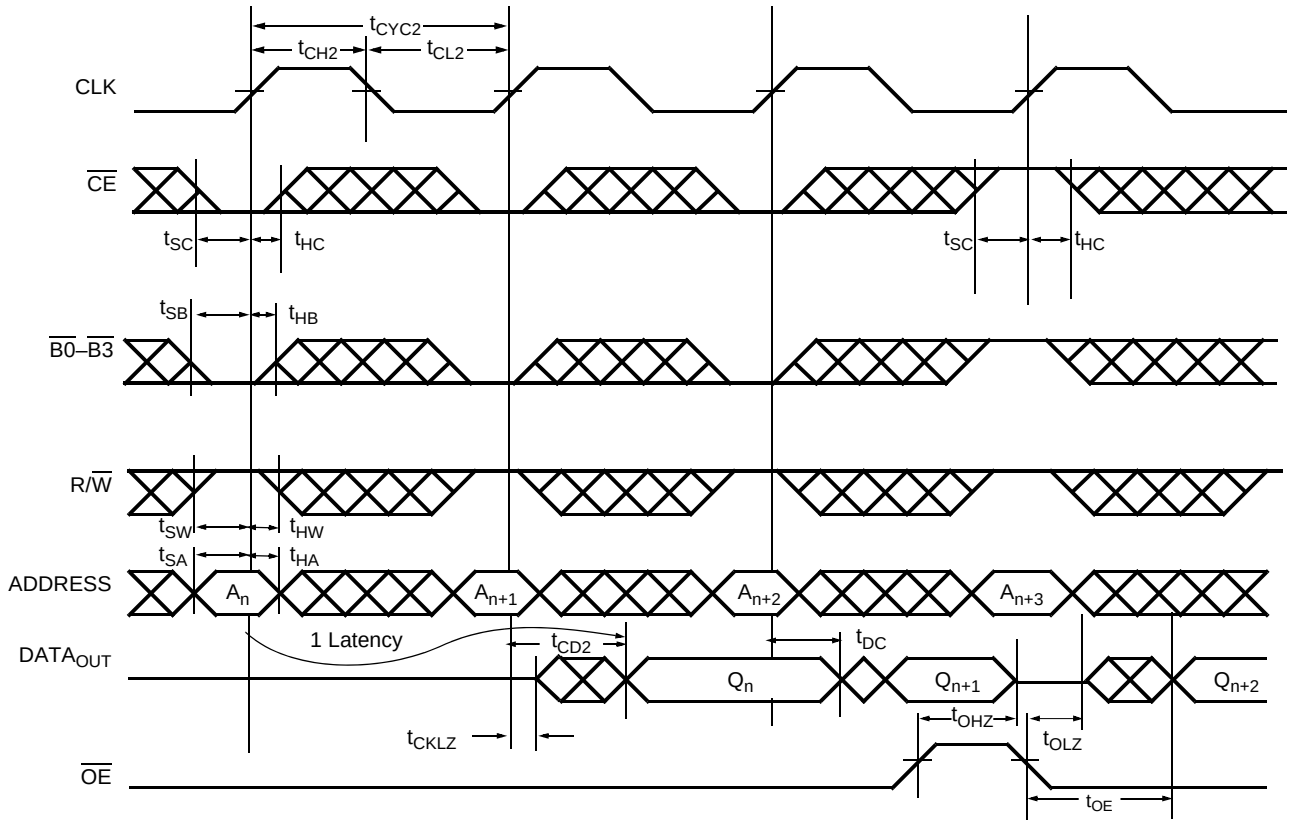


Figure 9. Read Cycle[26, 27, 28, 29, 30]



Notes

26. CE is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the CLK and can be deasserted after that. Data is out after the following CLK edge and is three-stated after the next CLK edge.
27. $\overline{OE}$ is asynchronously controlled; all other inputs (excluding $\overline{MRST}$ and JTAG) are synchronous to the rising clock edge.
28. ADS = CNTEN = LOW, and $\overline{MRST}$ = $\overline{CNTRST}$ = CNT/$\overline{MSK}$ = HIGH.
29. The output is disabled (high-impedance state) by $\overline{CE}$ = V_{IH} following the next rising edge of the clock.
30. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $\overline{CNTEN}$ = V_{IL} with CNT/$\overline{MSK}$ = V_{IH} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Figure 10. Bank Select Read[31, 32]

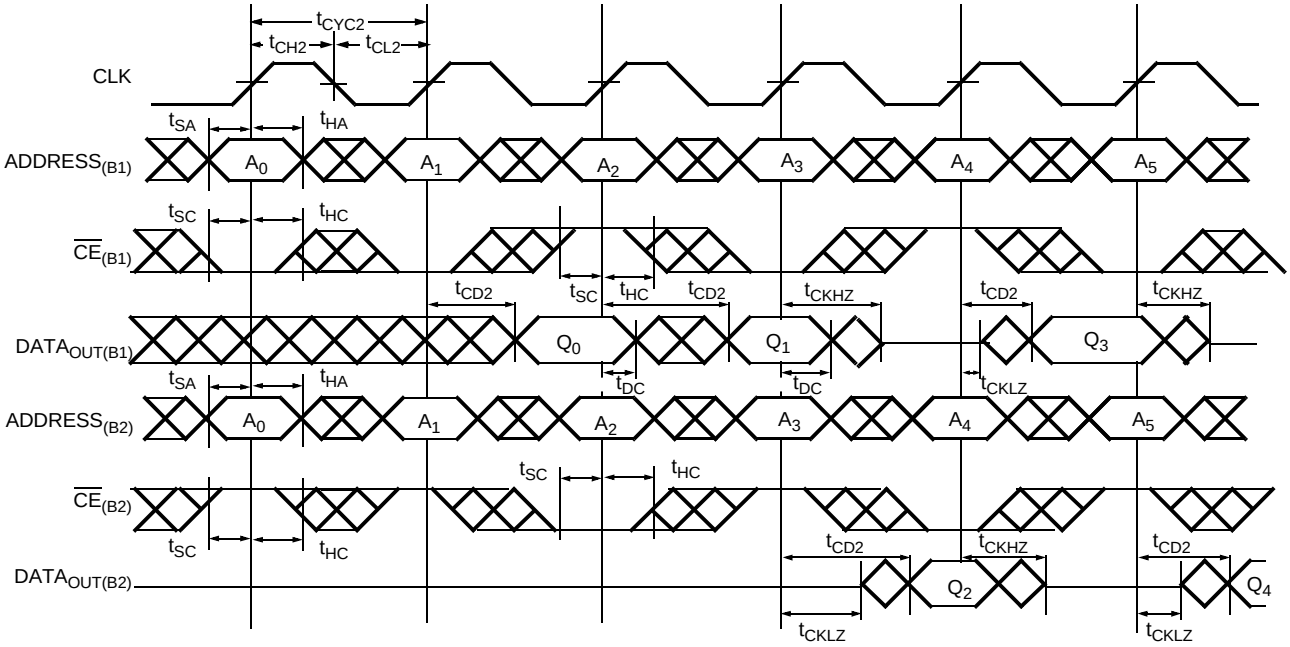
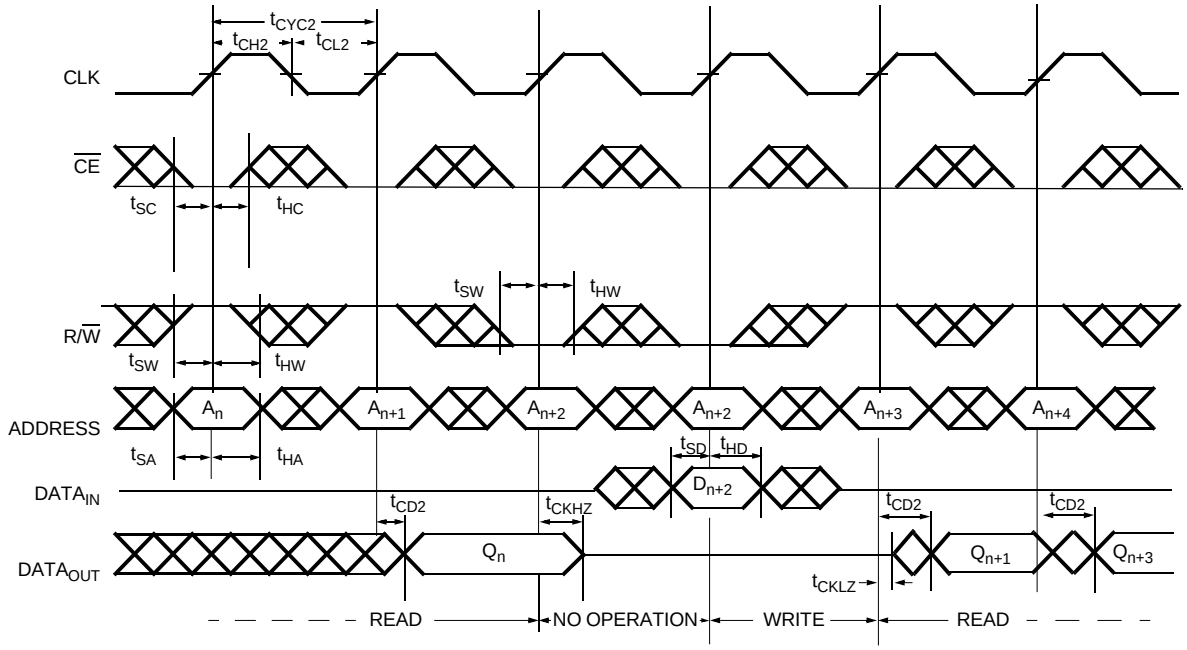


Figure 11. Read-to-Write-to-Read ($\overline{OE}$ = LOW)[30, 33, 34, 35, 36]



Notes

31. In this depth-expansion example, B1 represents Bank #1 and B2 is Bank #2; each bank consists of one Cypress CY7C0851V/CY7C0851AV/CY7C0852V/CY7C0852AV device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
32. $\overline{ADS}$ = $\overline{CNTEN}$= $\overline{B0}$ – $\overline{B3}$ = $\overline{OE}$ = LOW; $\overline{MRST}$ = $\overline{CNTRST}$ = CNT/$\overline{MSK}$ = HIGH.
33. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
34. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
35. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
36. $\overline{CE_0}$ = $\overline{B0}$ – $\overline{B3}$ = R/$\overline{W}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH. When R/$\overline{W}$ first switches low, since OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Figure 12. Read-to-Write-to-Read ($\overline{OE}$ Controlled)[37, 38, 39, 40]

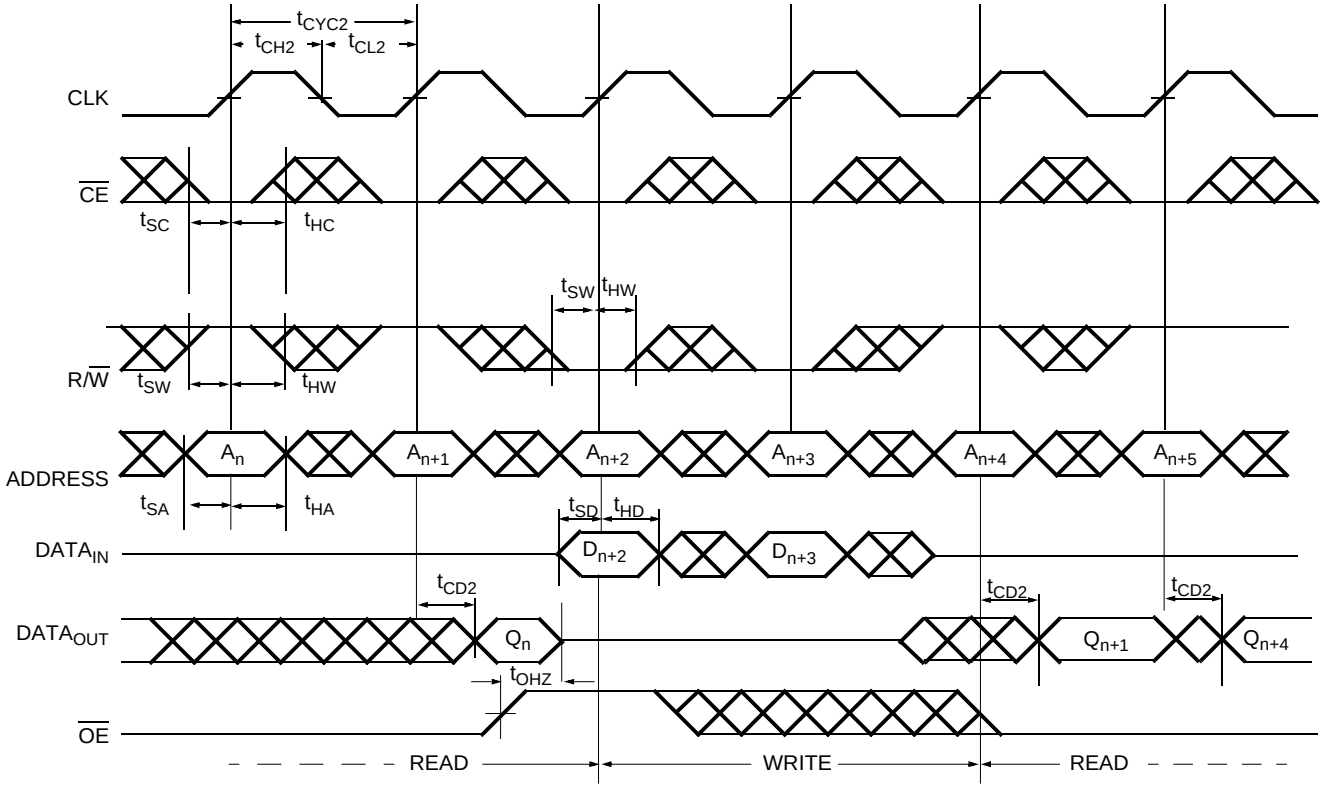
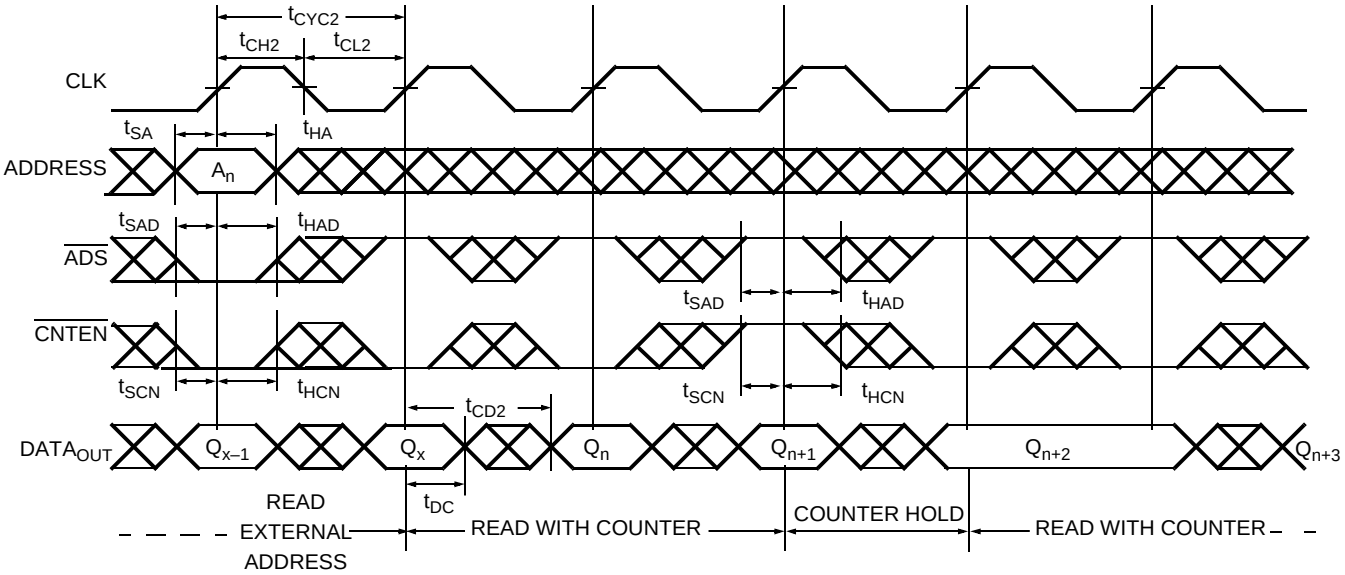


Figure 13. Read with Address Counter Advance[39]



Notes

37. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $\overline{CNTEN}$ = V_{IL} with CNT/$\overline{MSK}$ = V_{IH} constantly loads the address on the rising edge of the CLK. Numbers are for reference only
38. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
39. $\overline{CE}_0$ = $\overline{OE}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
40. $\overline{CE}_0$ = $\overline{B0}$ – $\overline{B3}$ = R/$\overline{W}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH. When R/$\overline{W}$ first switches low, since OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Figure 14. Write with Address Counter Advance [41]

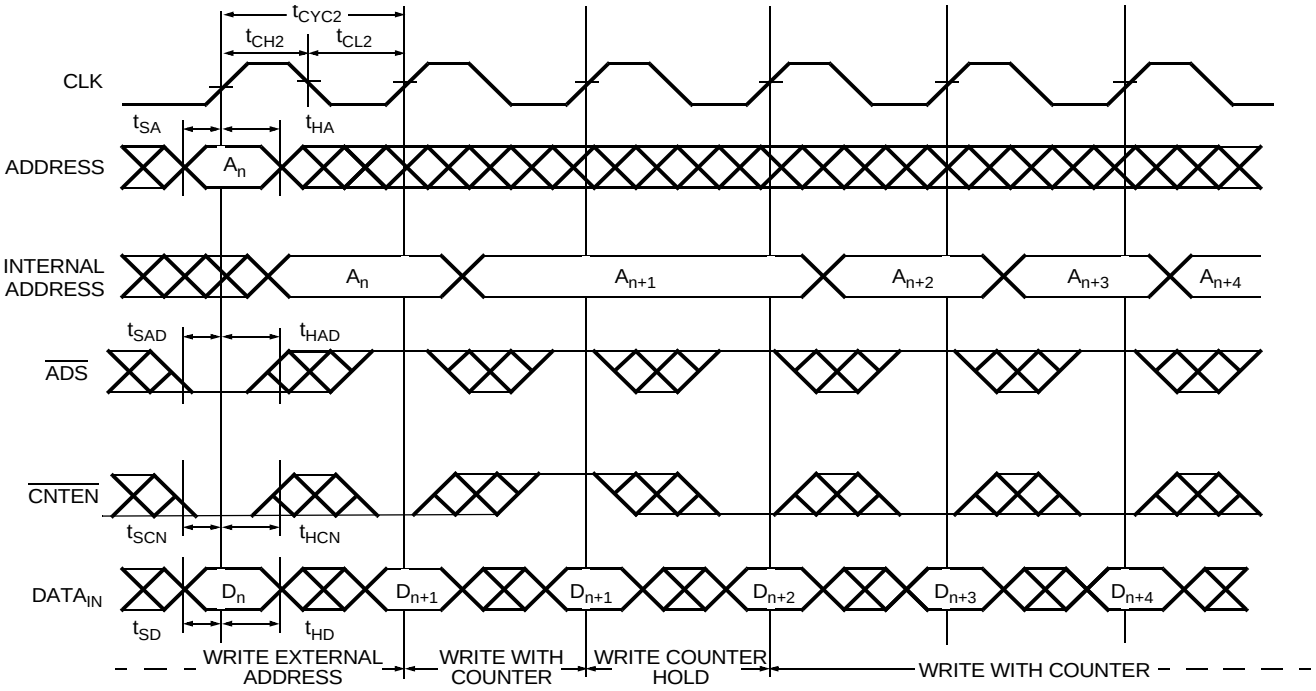
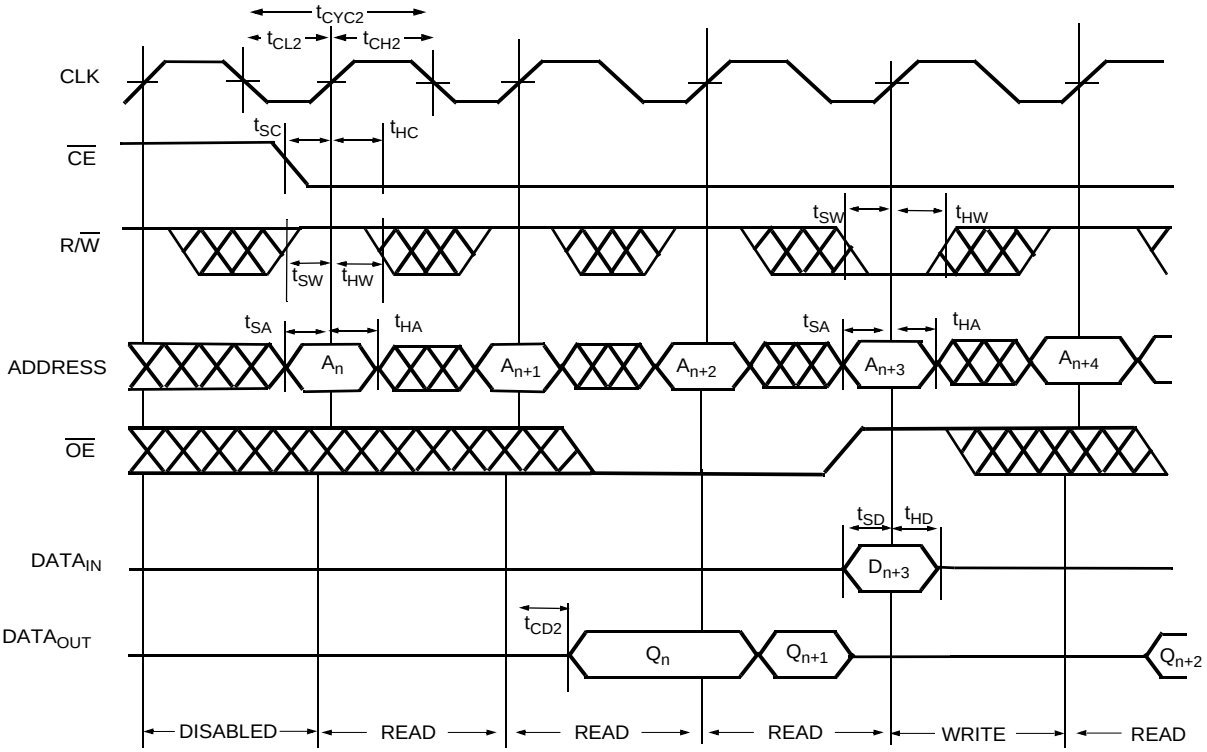


Figure 15. Disabled to Read-to-Read to Read-to-Write



Note

41. $\overline{CE_0}$ = $\overline{B0}$ – $\overline{B3}$ = R/$\overline{W}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH. When R/$\overline{W}$ first switches low, since OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Figure 16. Disabled to Write- to- Read to Write-to-Read

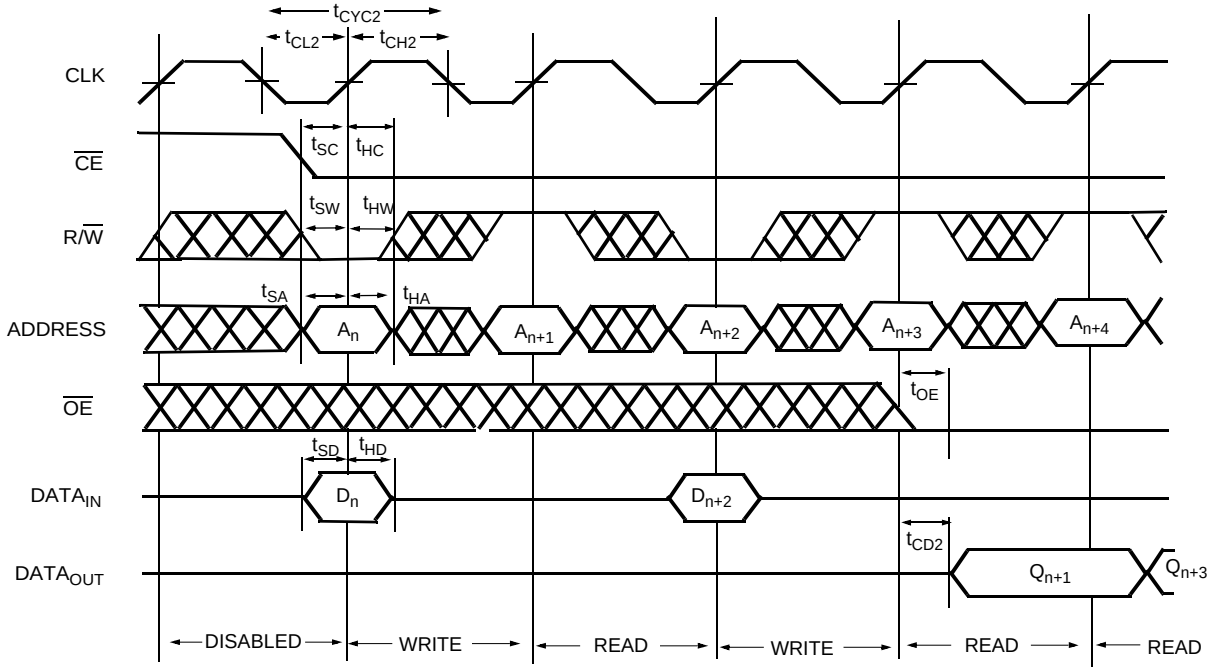
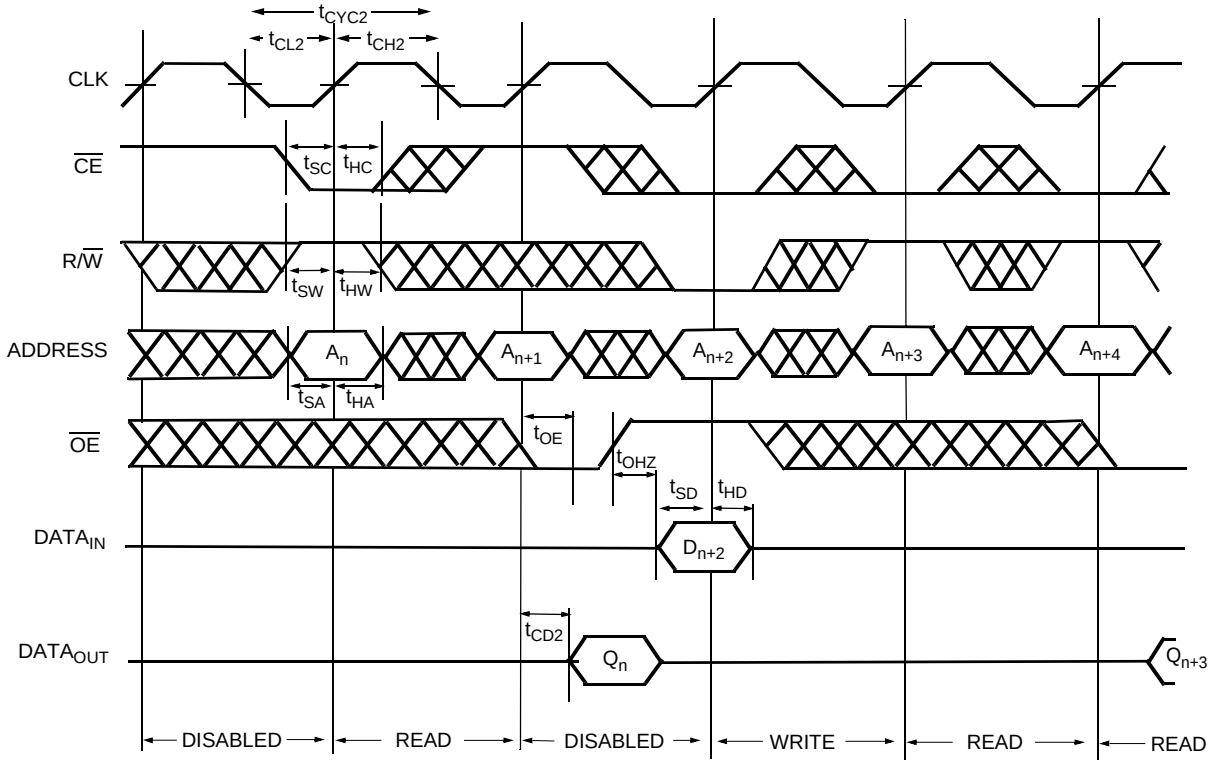
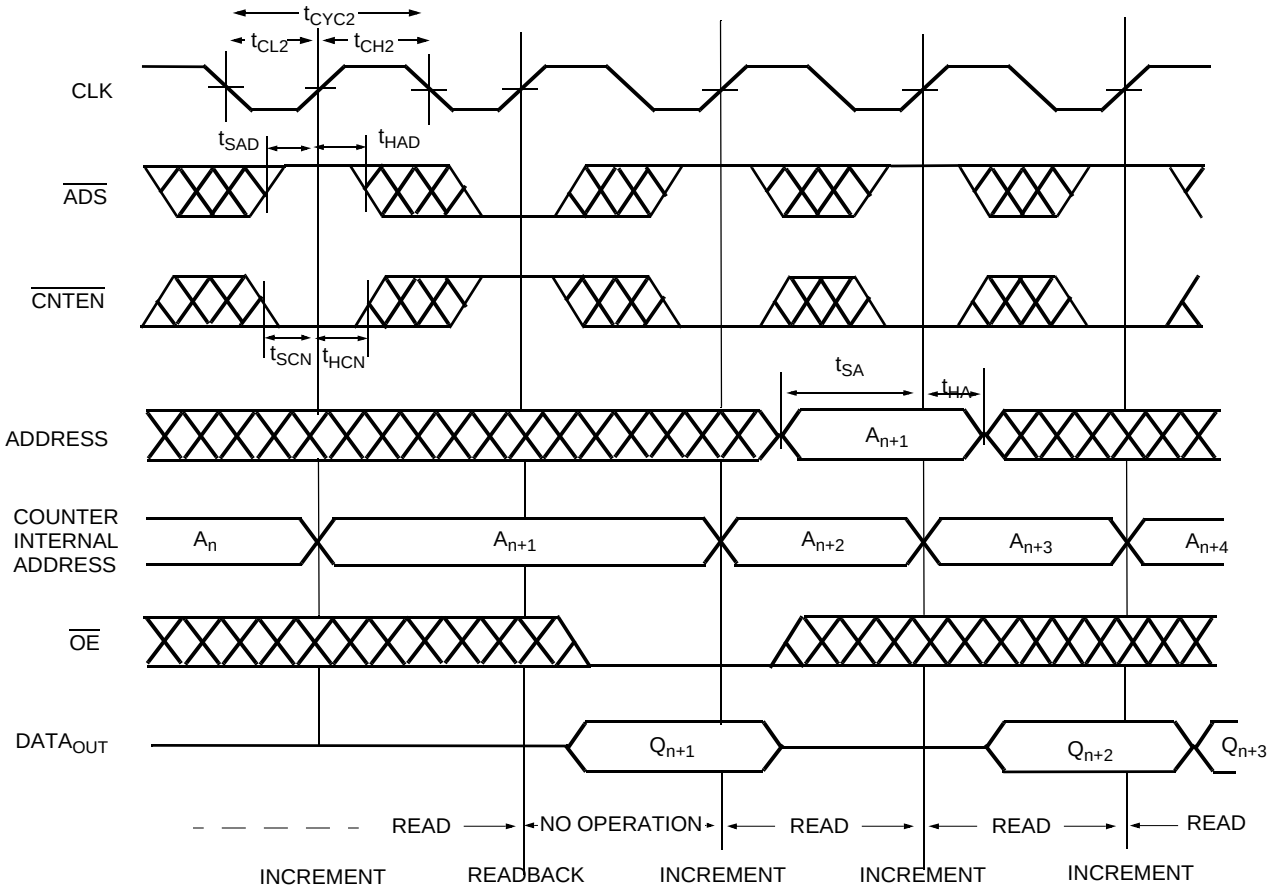


Figure 17. Disabled-to-Read to Disabled-to-Write



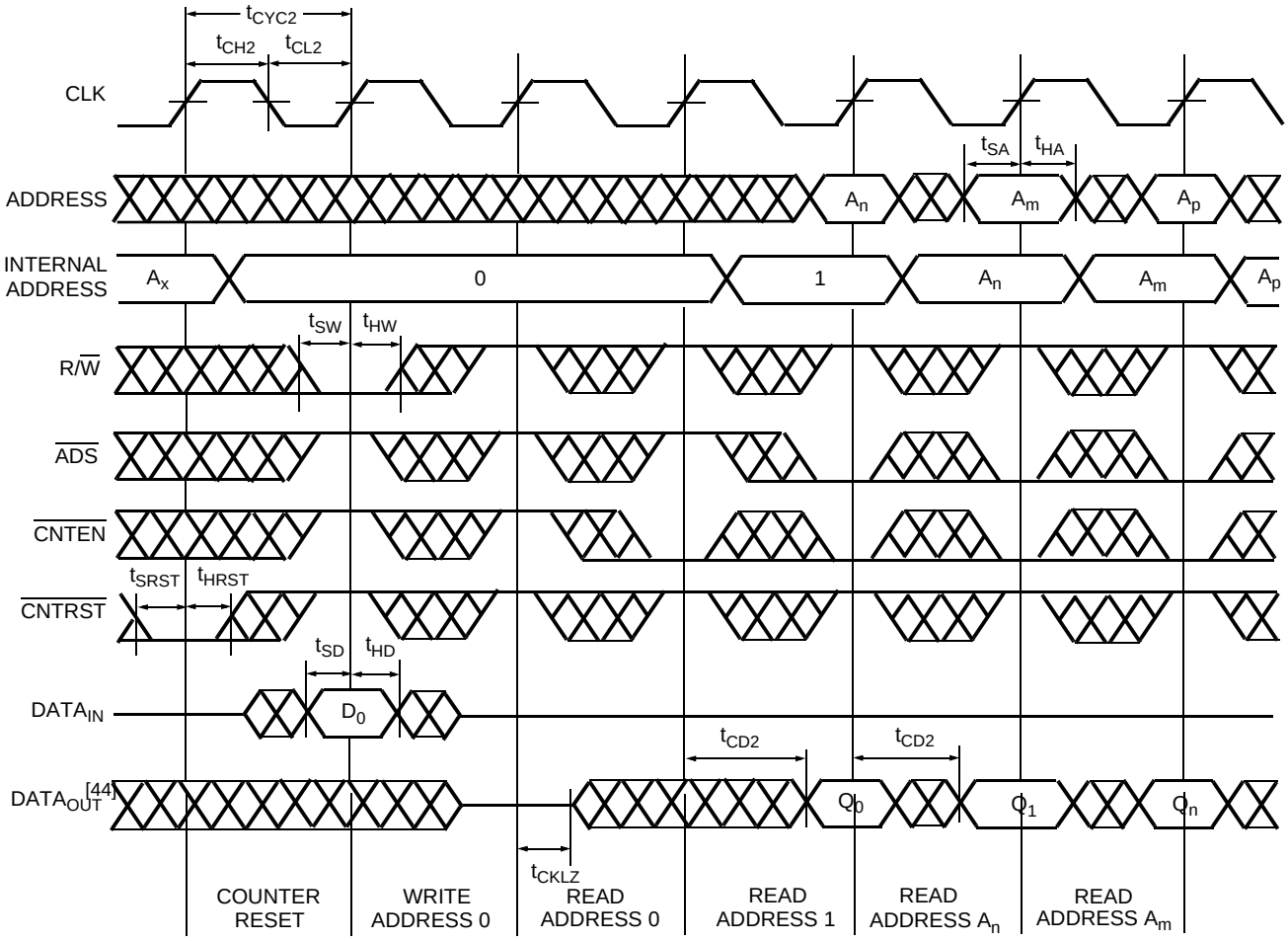
Switching Waveforms (continued)

Figure 18. Read-to-Readback to Read-to-Read (R/$\overline{W}$ = HIGH)



Switching Waveforms (continued)

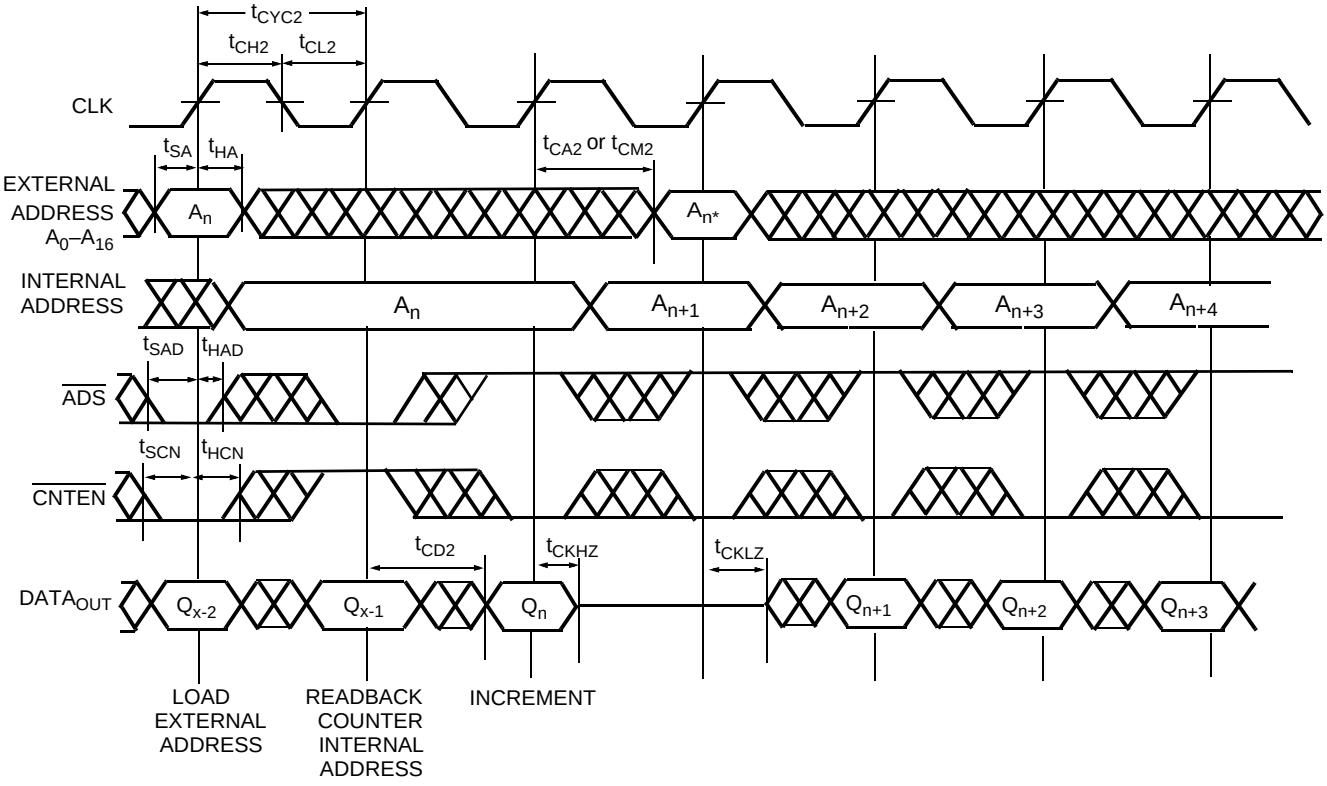
Figure 19. Counter Reset[42, 43, 44]



Notes
42. $\overline{CE_0}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
43. No dead cycle exists during counter reset. A Read or Write cycle may be coincidental with the counter reset.
44. Retransmit happens if the counter remains in increment mode after it wraps to initially loaded value.

Switching Waveforms (continued)

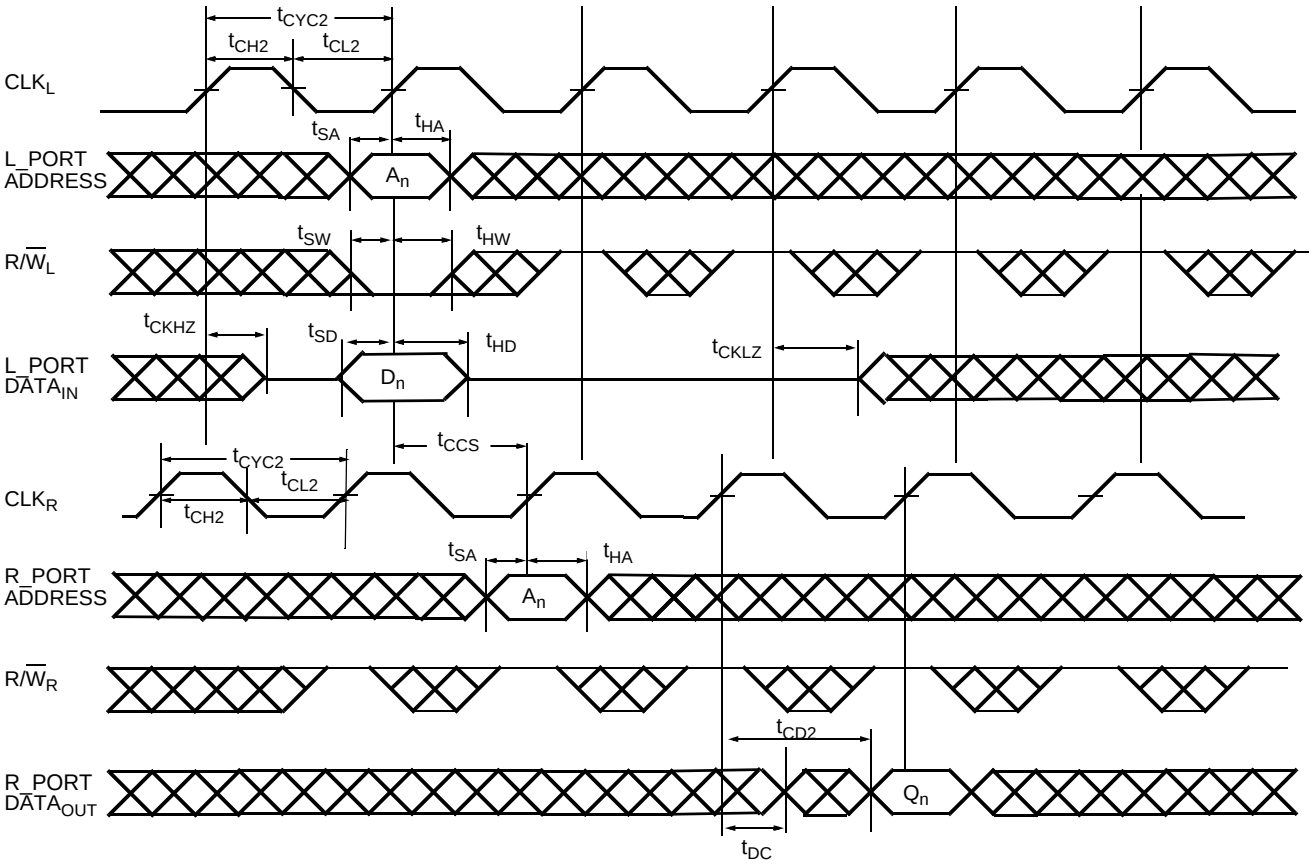
Figure 20. Readback State of Address Counter or Mask Register[45, 46, 47, 48]



Notes
45. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
46. Address in output mode. Host must not be driving address bus after t_{CKLZ} in next clock cycle.
47. Address in input mode. Host can drive address bus after t_{CKHZ}.
48. An * is the internal value of the address counter (or the mask register depending on the CNT/$\overline{MSK}$ level) being Read out on the address lines.

Switching Waveforms (continued)

Figure 21. Left_Port (L_Port) Write to Right_Port (R_Port) Read[49, 50, 51]

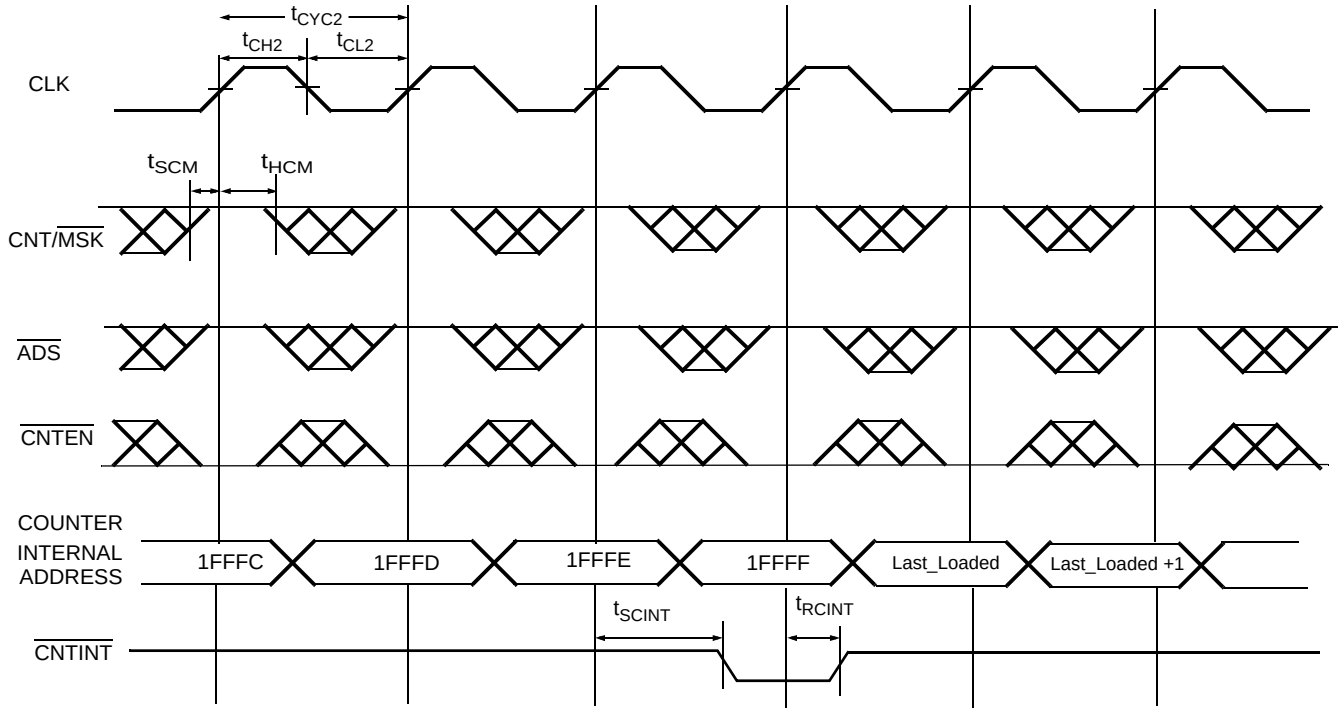


Notes

49. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
50. This timing is valid when one port is writing, and other port is reading the same location at the same time. If t_{CCS} is violated, indeterminate data is Read out.
51. If t_{CCS} < minimum specified value, then R_Port is Read the most recent data (written by L_Port) only (2 * t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock. If t_{CCS} ≥ minimum specified value, then R_Port is Read the most recent data (written by L_Port) (t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock.

Switching Waveforms (continued)

Figure 22. Counter Interrupt and Retransmit[52, 53, 54, 55, 56]



Notes
52. Retransmit happens if the counter remains in increment mode after it wraps to initially loaded value
53. $\overline{CE_0}$ = $\overline{OE}$ = B0 – B3 = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
54. $\overline{CNTINT}$ is always driven.
55. $\overline{CNTINT}$ goes LOW when the unmasked portion of the address counter is incremented to the maximum value.
56. The mask register assumed to have the value of 1FFFFh.

Switching Waveforms (continued)

Figure 23. MailBox Interrupt Timing[57, 58, 59, 60, 61]

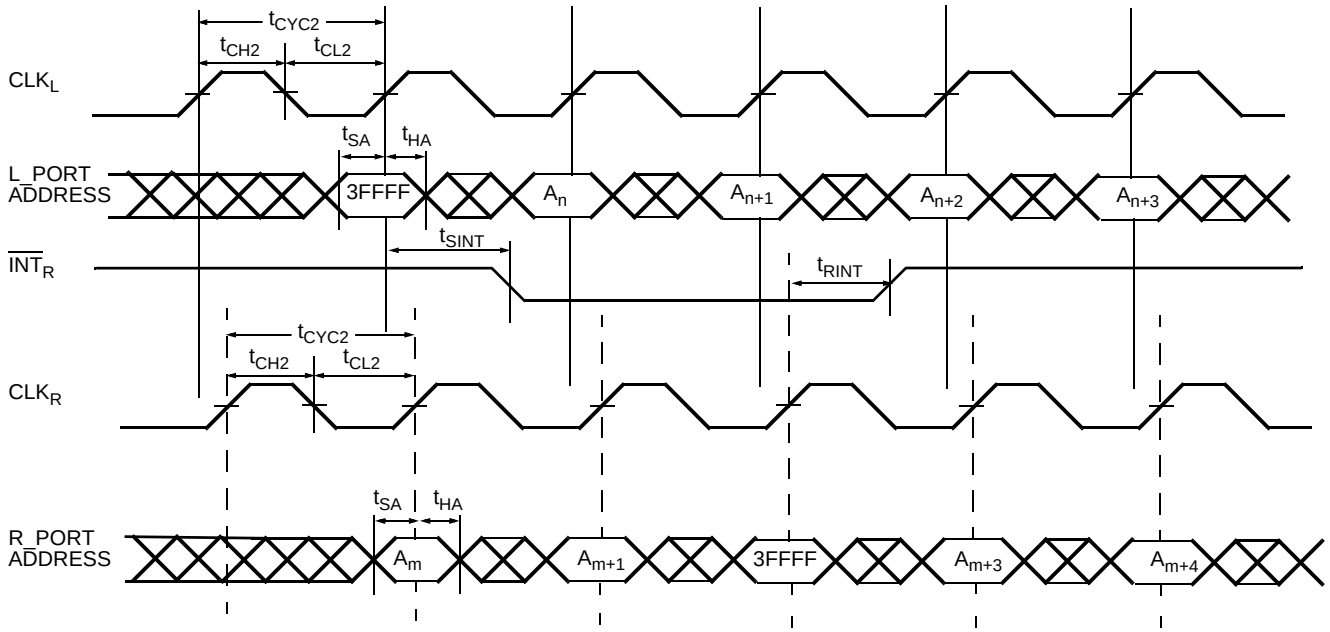


Table 7. Read/Write and Enable Operation (Any Port) [64, 65, 62, 63]

Inputs					Outputs	Operation
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	$DQ_0 - DQ_{35}$	
X	⎍	H	X	X	High-Z	Deselected
X	⎍	X	L	X	High-Z	Deselected
X	⎍	L	H	L	D_{IN}	Write
L	⎍	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs disabled

Notes
57. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
58. Address “3FFFF” is the mailbox location for R_Port of a 9M device.
59. L_Port is configured for Write operation, and R_Port is configured for Read operation.
60. At least one byte enable ($\overline{B0}$ – $\overline{B3}$) is required to be active during interrupt operations.
61. Interrupt flag is set with respect to the rising edge of the Write clock, and is reset with respect to the rising edge of the Read clock.
62. $\overline{OE}$ is an asynchronous input signal.
63. When $\overline{CE}$ changes state, deselection and Read happen after one cycle of latency.
64. 9 M device has 18 address bits, 4M device has 17 address bits, 2 M device has 16 address bits, and 1M device has 15 address bits.
65. “X” = “Don’t Care,” “H” = HIGH, “L” = LOW.

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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256K × 36 (9M) 3.3 V Synchronous CY7C0853V/CY7C0853AV Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C0853V-133BBI	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Industrial
	CY7C0853V-133BBXI		172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch (Pb-free)	
	CY7C0853V-133BBC	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Commercial
100	CY7C0853AV-100BBI	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Industrial
	CY7C0853V-100BBC	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Commercial

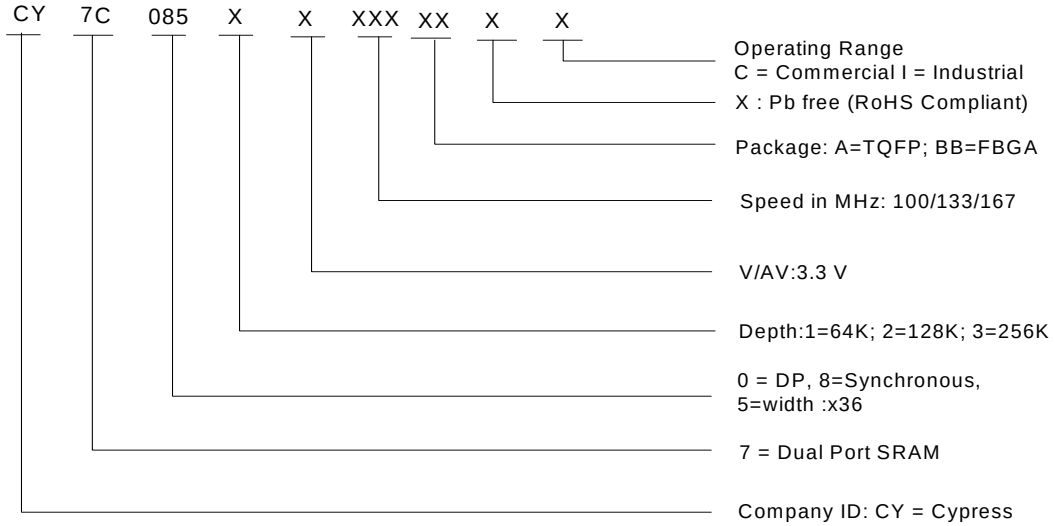
128K × 36 (4M) 3.3 V Synchronous CY7C0852AV/V Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
167	CY7C0852V-167BBC	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Commercial
	CY7C0852AV-167AXC	51-85132	176-Pin Thin Quad Flat Pack (24 x 24 x 1.4 mm) (Pb-free)	
133	CY7C0852AV-133AXC	51-85132	176-Pin Thin Quad Flat Pack (24 x 24 x 1.4 mm) (Pb-free)	
	CY7C0852AV-133BBI	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Industrial
	CY7C0852AV-133AXI	51-85132	176-Pin Thin Quad Flat Pack (24 x 24 x 1.4 mm) (Pb-free)	
	CY7C0852V-133BBC	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Commercial
	CY7C0852V-133BBI	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Industrial

64K × 36 (2M) 3.3V Synchronous CY7C0851AV/V Dual-Port SRAM

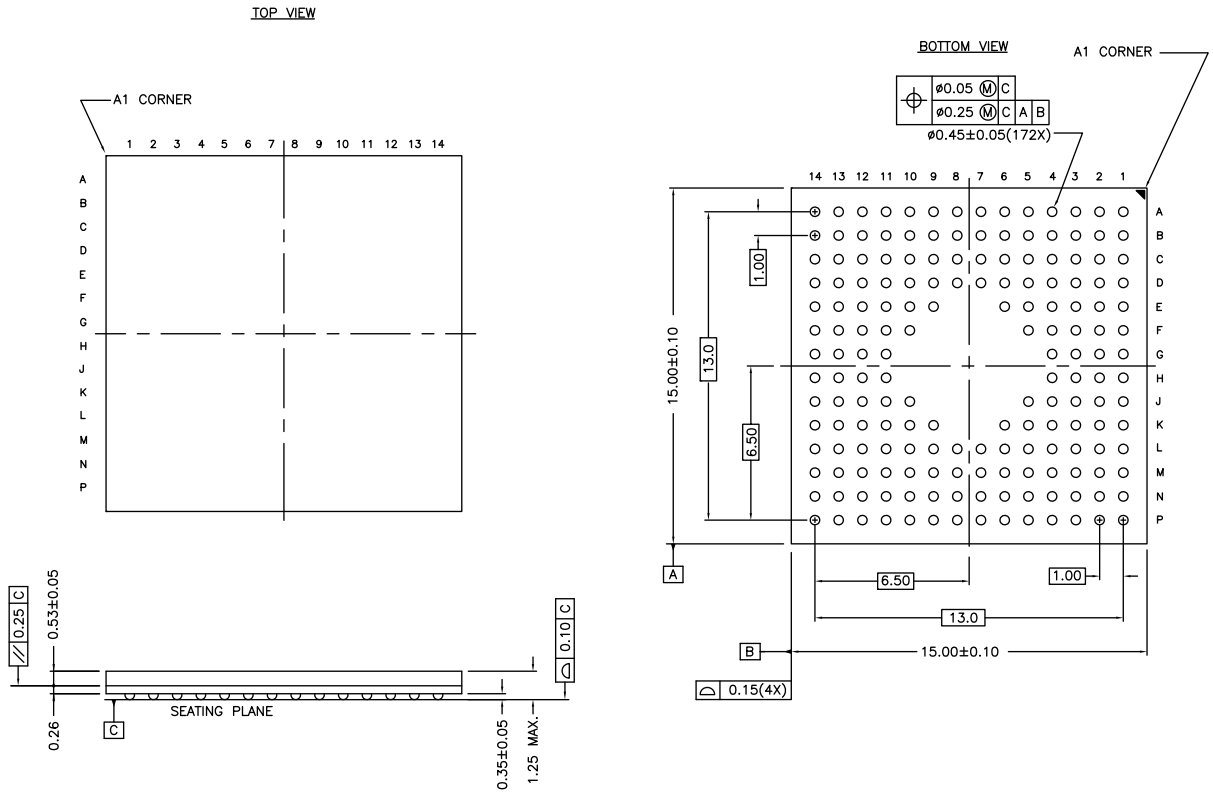
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
167	CY7C0851V-167BBC	51-85114	172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch	Commercial
	CY7C0851AV-167BBXC		172-Ball Grid Array (15 x 15 x 1.25 mm) with 1 mm pitch (Pb-free)	
133	CY7C0851AV-133AXI	51-85132	176-Pin Thin Quad Flat Pack (24 x 24 x 1.4 mm) (Pb-free)	Industrial
	CY7C0851AV-133BBI		176-Pin Thin Quad Flat Pack (24 x 24 x 1.4 mm) (Pb-free)	

Ordering Code Definition



Package Diagrams

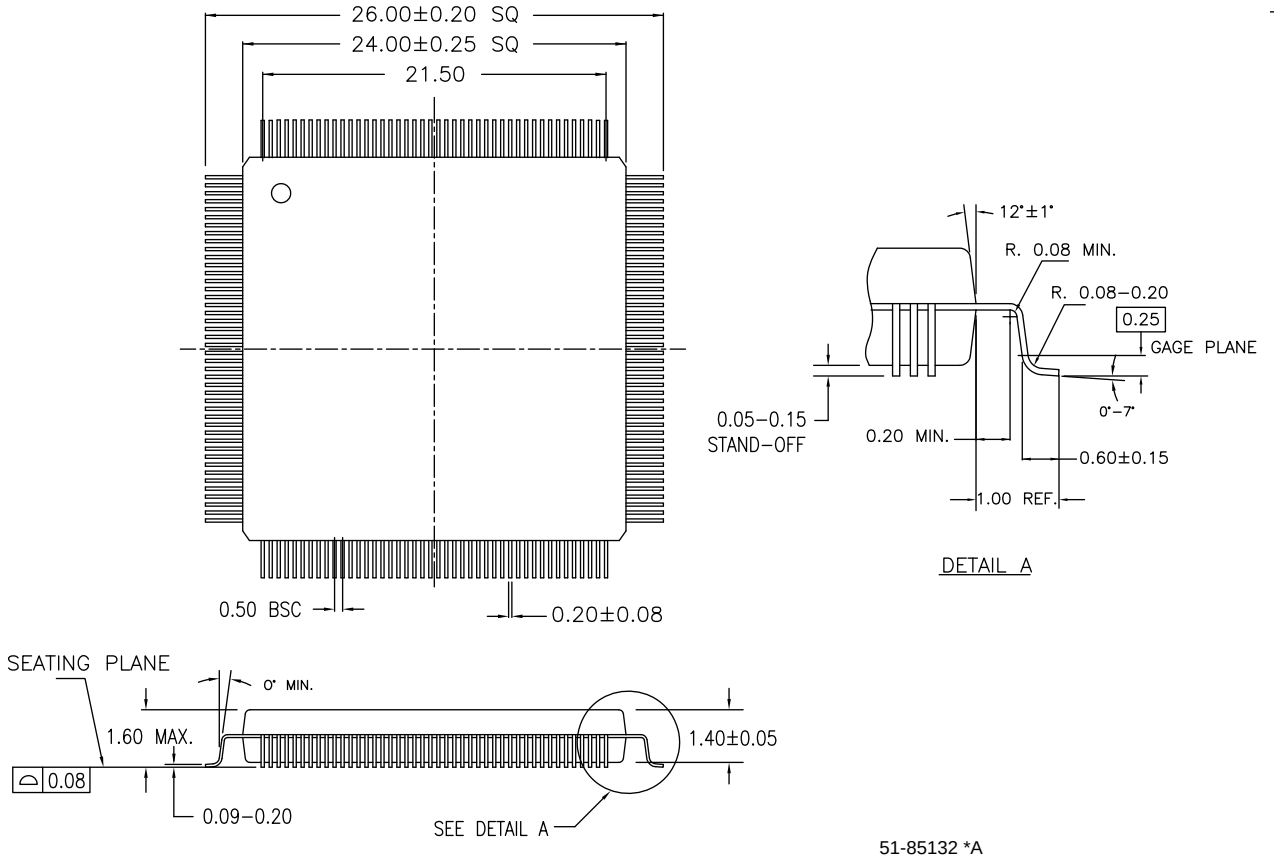
Figure 24. 172-Ball FBGA (15 x 15 x 1.25 mm) (51-85114)



51-85114 *D

Package Diagrams

Figure 25. 176-Pin Thin Quad Flat Pack (24 × 24 × 1.4 mm) (51-85132)



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
FBGA	fine-pitch ball grid array
I/O	input/output
JTAG	Joint Test Action Group
SRAM	static random access memory
TCK	test clock input
TDI	test data input
TDO	test data output
TQFP	thin quad plastic flatpack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	mega hertz
µA	microamperes
mA	milliamperes
mV	millivolts
ns	nanoseconds
Ω	ohms
pF	picofarad
V	volts
W	watts

Document History Page

Document Title: CY7C0850AV, CY7C0851V/CY7C0851AV, CY7C0852V/CY7C0852AV, CY7C0853V/CY7C0853AV, FLEx36™ 3.3V 32K/64K/128K/256K x 36 Synchronous Dual-Port RAM
Document Number: 38-06070

REV.	ECN NO.	Submis-sion Date	Orig. of Change	Description of Change
**	127809	08/04/03	SPN	This data sheet has been extracted from another data sheet: the 2M/4M/9M data sheet. The following changes have been made from the original as pertains to this device: Updated capacitance values Updated “Read-to-Write-to-Read (OE Controlled)” waveform Revised static discharge voltage Corrected 0853 pins L3 and L12 Added discussion of Pause/Restart for JTAG boundary scan Power up requirements added to Maximum Ratings information Revise t_{cd2}, t_{OE}, t_{OHZ}, t_{CKHZ}, t_{CKLZ} for the CY7C0853V to 4.7 ns Updated I_{cc} numbers Updated t_{HA}, t_{HB}, t_{HD} for -100 speed Separated out from the 4M data sheet Added 133-MHz Industrial device to Ordering Information table
*A	210948	See ECN	YDT	Changed mailbox addresses from 1FFFE and 1FFFF to 3FFFE and 3FFFF.
*B	216190	See ECN	YDT/Dcon	Corrected Revision of Document. CMS does not reflect this rev change
*C	231996	See ECN	YDT	Removed “A particular port can write to a certain location while another port is reading that location.” from Functional Description.
*D	238938	See ECN	WWZ	Merged 0853 (9Mx36) with 0852 (4Mx36) and 0851(2Mx36), add 0850 (1M x36), to the data sheet. Added product selection table. Added JTAG ID code for 1M device. Added note 14. Updated boundary scan section. Updated function description for the merge and addition.
*E	329122	See ECN	SPN	Updated Marketing part numbers
*F	389877	See ECN	KGH	Updated Read-to-Write-to-Read timing diagram to reflect accurate bus turnaround scheme. Added I_{SB5} Changed $t_{RSCNTINT}$ to 10ns Changed t_{RSF} to 10ns Added figure Disabled-to-Read-to-Read-to-Read-to-Write Added figure Disabled-to-Write-to-Read-to-Write-to-Read Added figure Disabled-to-Read-to-Disabled-to-Write Added figure Read-to-Readback-to-Read-to-Read ($R/\overline{W}$ = HIGH) Updated Read-to-Write-to-Read timing diagram to correct the data out schemes Updated Disabled-to-Read-to-Read-to-Read-to-Write timing diagram to correct the chip enable, data in, and data out schemes Updated Disabled-to-Write-to-Read-to-Write-to-Read timing diagram to correct the chip enable and output enable schemes Updated Disabled-to-Read-to-Disabled-to-Write timing diagram to correct the chip enable and output enable schemes
*G	391597	See ECN	SPN	Updated counter reset section to reflect mirror register behavior
*H	2544945	07/29/08	VKN/AESA	Updated Template. Updated ordering information
*I	2897087	03/22/10	RAME	Removed obsolete parts from ordering information table Updated package diagrams

Document History Page

Document Title: CY7C0850AV, CY7C0851V/CY7C0851AV, CY7C0852V/CY7C0852AV, CY7C0853V/CY7C0853AV, FLEx36™ 3.3V 32K/64K/128K/256K x 36 Synchronous Dual-Port RAM Document Number: 38-06070				
REV.	**ECN NO.**	**Submis-sion Date**	**Orig. of Change**	**Description of Change**
*J	3093275	11/23/2010	ADMU	Added new part CY7C0851AV-133BBI in the ordering information table Added information for parts CY7C0851V/CY7C0852V/CY7C0853V Updated as per new template Added Contents page Added Acronyms and Units of Measure table Added Ordering Code Definition
*K	3402163	10/12/2011	ADMU	Removed pruned parts CY7C0853AV-100BBC, CY7C0853AV-133BBC from Ordering Information Updated Package Diagrams.

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